FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11040-1E

*MEMORY*

**CMOS**

# 4 × 4 M × 4 BIT SYNCHRONOUS DYNAMIC RAM

# MB81F64442B-103E/-103/-10/-103L/-10L

**CMOS 4-Bank × 4,194,304-Word × 4 Bit**
**Synchronous Dynamic Random Access Memory**



## ■ DESCRIPTION

The Fujitsu MB81F64442B is a CMOS Synchronous Dynamic Random Access Memory (SDRAM) containing 67,108,864 memory cells accessible in a 4-bit format. The MB81F64442B features a fully synchronous operation referenced to a positive edge clock whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. The MB81F64442B SDRAM is designed to reduce the complexity of using a standard dynamic RAM (DRAM) which requires many control signal timing constraints, and may improve data bandwidth of memory as much as 5 times more than a standard DRAM.

The MB81F64442B is ideally suited for workstations, personal computers, laser printers, high resolution graphic adapters/accelerators and other applications where an extremely large memory and bandwidth are required and where a simple interface is needed.

## ■ PRODUCT LINE & FEATURES

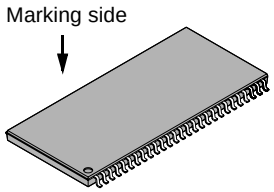
| Parameter | MB81F64442B | | | | |
|---|---|---|---|---|---|
| | -103E | -103 | -103L | -10 | -10L |
| CL - $t_{RCD}$ - $t_{RP}$ | 3 - 2 - 2 clk min. | | | 3 - 3 - 3 clk min. | |
| Clock Frequency | 100 MHz max. | | | 100 MHz max. | |
| Burst Mode Cycle Time | 10 ns min. | | | 10 ns min. | |
| Access Time From Clock (CL = 3) | 6 ns max. | | | 6 ns max. | |
| Operating Current (2 banks active) | 220 mA max. | | | 180 mA max. | |
| Power Down Mode Current ($I_{CC2P}$) | 3 mA max. | 2 mA max. | 1 mA max. | 2 mA max. | 1 mA max. |
| Self Refresh Current ($I_{CC6}$) | 2 mA max. | 1 mA max. | 500 µA max. | 1 mA max. | 500 µA max. |

- Single +3.3 V Supply ±0.3 V tolerance
- LVTTL compatible I/O
- 4 K refresh cycles every 65.6 ms
- Four bank operation
- Burst read/write operation and burst read/single write operation capability
- Standard and low power versions
- Programmable burst type, burst length, and CAS latency
- Auto-and Self-refresh (every 16 µs)
- CKE power down mode
- Output Enable and Input Data Mask

# MB81F64442B-103E/-103/-10/-103L/-10L

## ■ PACKAGE

Plastic TSOP(II) Package



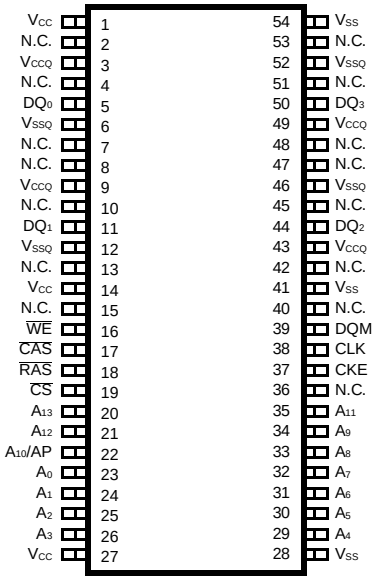

(FPT-54P-M02)
(Normal Bend)

**Package and Ordering Information**

– 54-pin plastic (400 mil) TSOP-II, order as MB81F64442B-×××FN (Std power), MB81F64442B-×××LFN (Low power), MB81F64442B-×××EFN (Extra power)

## ■ PIN ASSIGNMENTS AND DESCRIPTIONS

**54-Pin TSOP(II)**
(TOP VIEW)
<Normal Bend: FPT-54P-M02>




(Marking side)

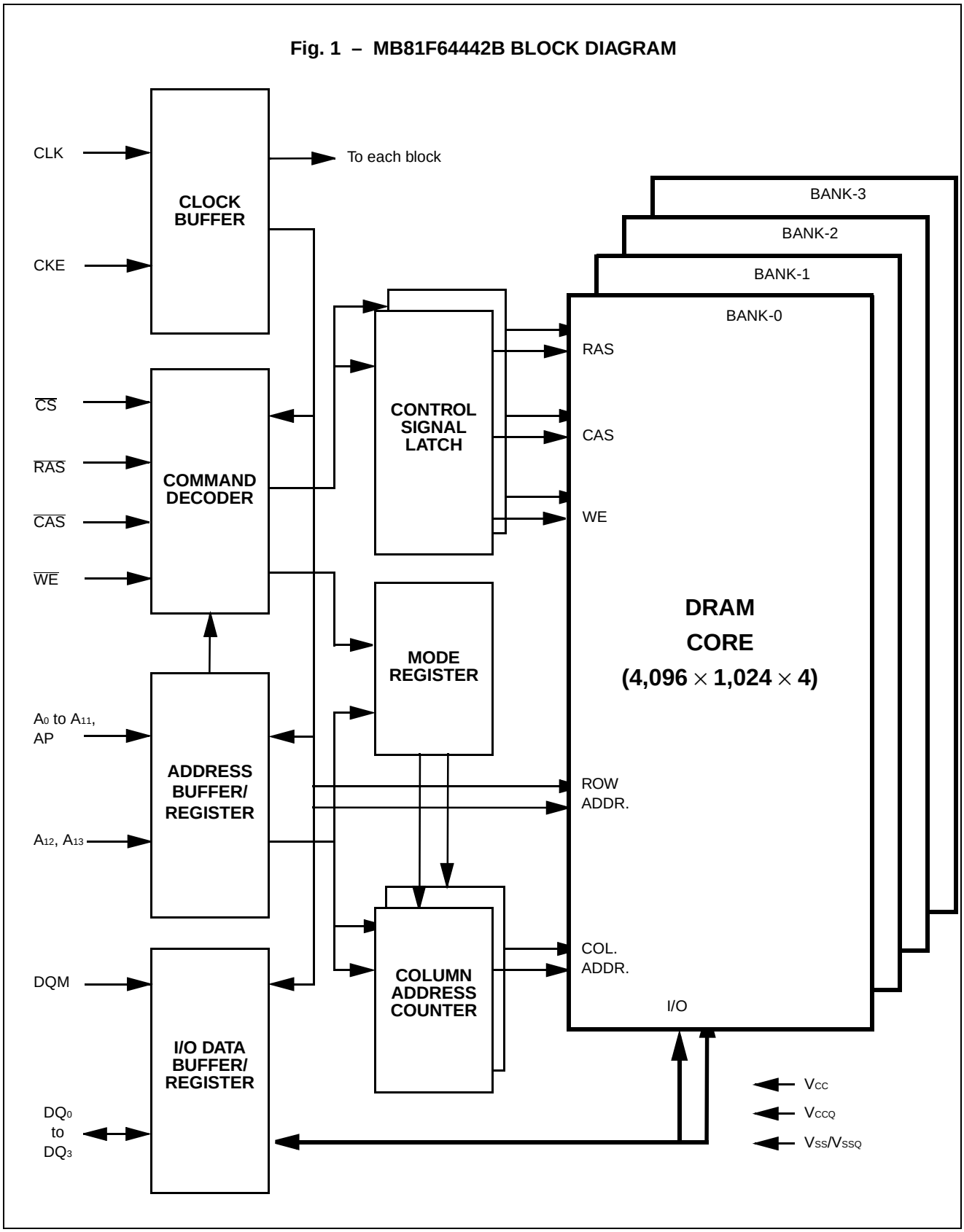
| Pin Number | Symbol | Function |
|---|---|---|
| 1, 3, 9, 14, 27, 43, 49 | $V_{CC}$, $V_{CCQ}$ | Supply Voltage |
| 5, 11, 44, 50 | $DQ_0$ to $DQ_3$ | Data I/O |
| 6, 12, 28, 41, 46, 52, 54 | $V_{SS}$, $V_{SSQ}$ * | Ground |
| 2, 4, 7, 8, 10, 13, 15, 36, 40, 42, 45, 47, 48, 51, 53 | N.C. | No Connection |
| 16 | $\overline{WE}$ | Write Enable |
| 17 | $\overline{CAS}$ | Column Address Strobe |
| 18 | $\overline{RAS}$ | Row Address Strobe |
| 19 | $\overline{CS}$ | Chip Select |
| 20, 21 | $A_{13}$ ($BA_0$), $A_{12}$ ($BA_1$) | Bank Select (Bank Address) |
| 22 | AP | Auto Precharge Enable |
| 22, 23, 24, 25, 26, 29, 30, 31, 32, 33, 34, 35 | $A_0$ to $A_{11}$ | Address Input • Row: $A_0$ to $A_{11}$ • Column: $A_0$ to $A_9$ |
| 37 | CKE | Clock Enable |
| 38 | CLK | Clock Input |
| 39 | DQM | Input Mask/Output Enable |

* : These pins are connected internally in the chip.

# MB81F64442B-103E/-103/-10/-103L/-10L

## ■ BLOCK DIAGRAM

Fig. 1 – MB81F64442B BLOCK DIAGRAM



## ■ FUNCTIONAL TRUTH TABLE Note 1

### COMMAND TRUTH TABLE Notes 2, 3, and 4

| Function | Notes | Symbol | CKE | | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | $A_{13}$, $A_{12}$ (BA) | $A_{10}$ (AP) | $A_{11}$ | $A_9$ to $A_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | n-1 | n | | | | | | | | |
| Device Deselect | *5 | DESL | H | X | H | X | X | X | X | X | X | X |
| No Operation | *5 | NOP | H | X | L | H | H | H | X | X | X | X |
| Burst Stop | | BST | H | X | L | H | H | L | X | X | X | X |
| Read | *6 | READ | H | X | L | H | L | H | V | L | X | V |
| Read with Auto-precharge | *6 | READA | H | X | L | H | L | H | V | H | X | V |
| Write | *6 | WRIT | H | X | L | H | L | L | V | L | X | V |
| Write with Auto-precharge | *6 | WRITA | H | X | L | H | L | L | V | H | X | V |
| Bank Active ($\overline{RAS}$) | *7 | ACTV | H | X | L | L | H | H | V | V | V | V |
| Precharge Single Bank | | PRE | H | X | L | L | H | L | V | L | X | X |
| Precharge All Banks | | PALL | H | X | L | L | H | L | X | H | X | X |
| Mode Register Set | *8, 9 | MRS | H | X | L | L | L | L | X | X | X | V |

**Notes:** *1. V = Valid, L = Logic Low, H = Logic High, X = either L or H.
*2. All commands assumes no CSUS command on previous rising edge of clock.
*3. All commands are assumed to be valid state transitions.
*4. All inputs are latched on the rising edge of clock.
*5. NOP and DESL commands have the same effect on the part.
*6. READ, READA, WRIT and WRITA commands should only be issued after the corresponding bank has been activated (ACTV command). Refer to STATE DIAGRAM.
*7. ACTV command should only be issued after corresponding bank has been precharged (PRE or PALL command).
*8. Required after power up.
*9. MRS command should only be issued after all banks have been precharged (PRE or PALL command). Refer to STATE DIAGRAM.

## DQM TRUTH TABLE

| Function | Command | CKE | | DQM |
|---|---|---|---|---|
| | | n-1 | n | |
| Data Write/Output Enable | ENBL | H | X | L |
| Data Mask/Output Disable | MASK | H | X | H |

## CKE TRUTH TABLE

| Current State | Function | Notes | Symbol | CKE | | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | $A_{13}$, $A_{12}$ (BA) | $A_{10}$ (AP) | $A_{11}$, $A_{9-0}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | n-1 | n | | | | | | | |
| Bank Active | Clock Suspend Mode Entry | *1 | CSUS | H | L | X | X | X | X | X | X | X |
| Any (Except Idle) | Clock Suspend Continue | *1 | | L | L | X | X | X | X | X | X | X |
| Clock Suspend | Clock Suspend Mode Exit | | | L | H | X | X | X | X | X | X | X |
| Idle | Auto-refresh Command | *2 | REF | H | H | L | L | L | H | X | X | X |
| Idle | Self-refresh Entry | *2, 3 | SELF | H | L | L | L | L | H | X | X | X |
| Self Refresh | Self-refresh Exit | *4 | SELFX | L | H | L | H | H | H | X | X | X |
| | | | | L | H | H | X | X | X | X | X | X |
| Idle | Power Down Entry | *3 | PD | H | L | L | H | H | H | X | X | X |
| | | | | H | L | H | X | X | X | X | X | X |
| Power Down | Power Down Exit | | | L | H | L | H | H | H | X | X | X |
| | | | | L | H | H | X | X | X | X | X | X |

**Notes:** *1. The CSUS command requires that at least one bank is active. Refer to STATE DIAGRAM.
*2. REF and SELF commands should only be issued after all banks have been precharged (PRE or PALL command). Refer to STATE DIAGRAM.
*3. SELF and PD commands should only be issued after the last read data have been appeared on DQ.
*4. CKE should be held high within $t_{RC}$.

**OPERATION COMMAND TABLE (Applicable to single bank)**

| Current State | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Addr | Command | Function | Notes |
|---|---|---|---|---|---|---|---|---|
| Idle | H | X | X | X | X | DESL | NOP | |
| | L | H | H | H | X | NOP | NOP | |
| | L | H | H | L | X | BST | NOP | |
| | L | H | L | H | BA, CA, AP | READ/READA | Illegal | *2 |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Illegal | *2 |
| | L | L | H | H | BA, RA | ACTV | Bank Active | |
| | L | L | H | L | BA, AP | PRE/PALL | NOP (PALL may affect other banks.) | |
| | L | L | L | H | X | REF/SELF | Auto-refresh or Self-refresh | *3 |
| | L | L | L | L | MODE | MRS | Mode Register Set (Idle after $t_{RSC}$) | *3, 7 |
| Bank Active | H | X | X | X | X | DESL | NOP | |
| | L | H | H | H | X | NOP | NOP | |
| | L | H | H | L | X | BST | NOP | |
| | L | H | L | H | BA, CA, AP | READ/READA | Begin Read; Determine AP | |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Begin Write; Determine AP | |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA, AP | PRE/PALL | Precharge; Determine Precharge Type (PALL may affect other banks.) | |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |

*(Continued)*

| Current State | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Addr | Command | Function | Notes |
|---|---|---|---|---|---|---|---|---|
| Read | H | X | X | X | X | DESL | NOP (Continue Burst to End → Bank Active) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to End → Bank Active) | |
| | L | H | H | L | X | BST | Burst Stop → Bank Active | |
| | L | H | L | H | BA, CA, AP | READ/READA | Terminate Burst, New Read; Determine AP | |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Terminate Burst, Start Write; Determine AP | *4 |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA, AP | PRE/PALL | Terminate Burst, Precharge → Idle; Determine Precharge Type | |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |
| Write | H | X | X | X | X | DESL | NOP (Continue Burst to End → Bank Active) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to End → Bank Active) | |
| | L | H | H | L | X | BST | Burst Stop → Bank Active | |
| | L | H | L | H | BA, CA, AP | READ/READA | Terminate Burst, Start Read; Determine AP | |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Terminate Burst, New Write; Determine AP | |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA, AP | PRE/PALL | Terminate Burst, Precharge → Idle; Determine Precharge Type (PALL may affect other banks.) | *4 |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |

*(Continued)*

| Current State | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Addr | Command | Function | Notes |
|---|---|---|---|---|---|---|---|---|
| Read with Auto-precharge | H | X | X | X | X | DESL | NOP (Continue Burst to End → Precharge → Idle) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to End → Precharge → Idle) | |
| | L | H | H | L | X | BST | Illegal | |
| | L | H | L | H | BA, CA, AP | READ/READA | Illegal | |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Illegal | |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA | PRE | Illegal | *2 |
| | L | L | H | L | AP | PALL | Illegal | |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |
| Write with Auto-precharge | H | X | X | X | X | DESL | NOP (Continue Burst to End → Precharge → Idle) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to End → Precharge → Idle) | |
| | L | H | H | L | X | BST | Illegal | |
| | L | H | L | H | BA, CA, AP | READ/READA | Illegal | |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Illegal | |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA | PRE | Illegal | *2 |
| | L | L | H | L | AP | PALL | Illegal | |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |

*(Continued)*

| Current State | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Addr | Command | Function | Notes |
|---|---|---|---|---|---|---|---|---|
| Precharge | H | X | X | X | X | DESL | NOP (Idle after $t_{RP}$) | |
| | L | H | H | H | X | NOP | NOP (Idle after $t_{RP}$) | |
| | L | H | H | L | X | BST | NOP (Idle after $t_{RP}$) | |
| | L | H | L | H | BA, CA, AP | READ/READA | Illegal | *2 |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Illegal | *2 |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA, AP | PRE/PALL | NOP (PALL may affect other bank) | *5 |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |
| Bank Activating | H | X | X | X | X | DESL | NOP (Bank Active after $t_{RCD}$) | |
| | L | H | H | H | X | NOP | NOP (Bank Active after $t_{RCD}$) | |
| | L | H | H | L | X | BST | NOP (Bank Active after $t_{RCD}$) | |
| | L | H | L | H | BA, CA, AP | READ/READA | Illegal | *2 |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Illegal | *2 |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2, 8 |
| | L | L | H | L | BA | PRE | Illegal | *2 |
| | L | L | H | L | AP | PALL | Illegal | |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |

*(Continued)*

*(Continued)*

| Current State | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Addr | Command | Function | Notes |
|---|---|---|---|---|---|---|---|---|
| Refreshing | H | X | X | X | X | DESL | NOP (Idle after $t_{RC}$) | |
| | L | H | H | X | X | NOP/BST | NOP (Idle after $t_{RC}$) | |
| | L | H | L | X | X | READ/READA/ WRIT/WRITA | Illegal | |
| | L | L | H | X | X | ACTV/ PRE/PALL | Illegal | |
| | L | L | L | X | X | REF/SELF/ MRS | Illegal | |
| Mode Register Setting | H | X | X | X | X | DESL | NOP (Idle after $t_{RSC}$) | |
| | L | H | H | H | X | NOP | NOP (Idle after $t_{RSC}$) | |
| | L | H | H | L | X | BST | Illegal | |
| | L | H | L | X | X | READ/READA/ WRIT/WRITA | Illegal | |
| | L | L | X | X | X | ACTV/PRE/ PALL/REF/ SELF/MRS | Illegal | |

ABBREVIATIONS:

RA = Row Address BA = Bank Address
CA = Column Address AP = Auto Precharge

## COMMAND TRUTH TABLE FOR CKE

| Current State | CKE n-1 | CKE n | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Addr | Function | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Self-refresh | H | X | X | X | X | X | X | Invalid | |
| | L | H | H | X | X | X | X | Exit Self-refresh (Self-refresh Recovery → Idle after $t_{RC}$) | |
| | L | H | L | H | H | H | X | Exit Self-refresh (Self-refresh Recovery → Idle after $t_{RC}$) | |
| | L | H | L | H | H | L | X | Illegal | |
| | L | H | L | H | L | X | X | Illegal | |
| | L | H | L | L | X | X | X | Illegal | |
| | L | L | X | X | X | X | X | NOP (Maintain Self-refresh) | |
| Self-refresh Recovery | L | X | X | X | X | X | X | Invalid | |
| | H | H | H | X | X | X | X | Idle after $t_{RC}$ | |
| | H | H | L | H | H | H | X | Idle after $t_{RC}$ | |
| | H | H | L | H | H | L | X | Illegal | |
| | H | H | L | H | L | X | X | Illegal | |
| | H | H | L | L | X | X | X | Illegal | |
| | H | L | X | X | X | X | X | Illegal | |

*(Continued)*

| Current State | CKE n-1 | CKE n | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Addr | Function | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Power Down | H | X | X | X | X | X | X | Invalid | |
| | L | H | H | X | X | X | X | Exit Power Down Mode → Idle | |
| | | | L | H | H | H | X | | |
| | L | L | X | X | X | X | X | NOP (Maintain Power Down Mode) | |
| | L | H | L | L | X | X | X | Illegal | |
| | L | H | L | H | L | X | X | Illegal | |
| | L | H | L | H | H | L | X | Illegal | |
| All Banks Idle | H | H | H | X | X | X | | Refer to the Operation Command Table. | |
| | H | H | L | H | X | X | | Refer to the Operation Command Table. | |
| | H | H | L | L | H | X | | Refer to the Operation Command Table. | |
| | H | H | L | L | L | H | X | Auto-refresh | |
| | H | H | L | L | L | L | MODE | Refer to the Operation Command Table. | |
| | H | L | H | X | X | X | X | Power Down | *6 |
| | H | L | L | H | H | H | X | Power Down | *6 |
| | H | L | L | H | H | L | | Illegal | |
| | H | L | L | H | L | X | X | Illegal | |
| | H | L | L | L | H | X | X | Illegal | |
| | H | L | L | L | L | H | X | Self-refresh | *6 |
| | H | L | L | L | L | L | X | Illegal | |
| | L | X | X | X | X | X | X | Invalid | |

*(Continued)*

*(Continued)*

| Current State | CKE n-1 | CKE n | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Addr | Function | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Bank Active Bank Activating Read/Write<br><br>Read with Auto-precharge/ Write with Auto-precharge | H | H | X | X | X | X | X | Refer to the Operation Command Table. | |
| | H | L | X | X | X | X | X | Begin Clock Suspend next cycle | |
| | L | H | X | X | X | X | X | Exit Clock Suspend next cycle | |
| | L | L | X | X | X | X | X | Maintain Clock Suspend | |
| Clock Suspend | H | X | X | X | X | X | X | Invalid | |
| | L | H | X | X | X | X | X | Exit Clock Suspend next cycle | |
| | L | L | X | X | X | X | X | Maintain Clock Suspend | |
| Any State Other Than Listed Above | L | X | X | X | X | X | X | Invalid | |
| | H | H | X | X | X | X | X | Refer to the Operation Command Table. | |
| | H | L | X | X | X | X | X | Illegal | |

**Notes:** *1. All entries assume the CKE was High during the proceeding clock cycle and the current clock cycle.
Illegal means don't used command. If used, power up sequence be asserted after power shut down.

*2. Illegal to bank in specified state; entry may be legal in the bank specified by BA, depending on the state of that bank.

*3. Illegal if any bank is not idle.

*4. Must satisfy bus contention, bus turn around, and/or write recovery requirements.

*5. NOP to bank precharging or in idle state.
May precharge bank spesified by BA (and AP).

*6. SELF command should only be issued after the last read data have been appeared on DQ.

*7. MRS command should only be issued on condition that all DQ are in Hi-Z.

## ■ FUNCTIONAL DESCRIPTION

### SDRAM BASIC FUNCTION

Three major differences between this SDRAM and conventional DRAMs are: synchronized operation, burst mode, and mode register.

The **synchronized operation** is the fundamental difference. An SDRAM uses a clock input for the synchronization, where the DRAM is basically asynchronous memory although it has been using two clocks, $\overline{RAS}$ and $\overline{CAS}$. Each operation of DRAM is determined by their timing phase differences while each operation of SDRAM is determined by commands and all operations are referenced to a positive clock edge. Fig 3 shows the basic timing diagram differences between SDRAMs and DRAMs.

The **burst mode** is a very high speed access mode utilizing an internal column address generator. Once a column addresses for the first access is set, following addresses are automatically generated by the internal column address counter.

The **mode registe**r is to justify the SDRAM operation and function into desired system conditions. MODE REGISTER TABLE shows how SDRAM can be configured for system requirement by mode register programming.

### CLOCK (CLK) and CLOCK ENABLE (CKE)

All input and output signals of SDRAM use register type buffers. A CLK is used as a trigger for the register and internal burst counter increment. All inputs are latched by a positive edge of CLK. All outputs are validated by the CLK. CKE is a high active clock enable signal. When CKE = Low is latched at a clock input during active cycle, the next clock will be internally masked. During idle state (all banks have been precharged), the Power Down mode (standby) is entered with CKE = Low and this will make extremely low standby current.

### CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ enables all commands inputs, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$, and address input. When $\overline{CS}$ is High, command signals are negated but internal operation such as burst cycle will not be suspended. If such a control isn't needed, $\overline{CS}$ can be tied to ground level.

### COMMAND INPUT ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$)

Unlike a conventional DRAM, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ do not directly imply SDRAM operation, such as Row address strobe by $\overline{RAS}$. Instead, each combination of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ input in conjunction with $\overline{CS}$ input at a rising edge of the CLK determines SDRAM operation. Refer to FUNCTIONAL TRUTH TABLE in page 5.

### ADDRESS INPUT ($A_0$ to $A_{11}$)

Address input selects an arbitrary location of a total of 4,194,304 words of each memory cell matrix. A total of fourteen address input signals are required to decode such a matrix. SDRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV), twelve Row addresses are initially latched and the remainder of ten Column addresses are then latched by a Column address strobe command of either a Read command (READ or READA) or Write command (WRIT or WRITA).

### BANK SELECT ($A_{13}$, $A_{12}$)

This SDRAM has four banks and each bank is organized as 4 M words by 4-bit.
Bank selection by $A_{13}$, $A_{12}$ occurs at Bank Active command (ACTV) followed by read (READ or READA), write (WRIT or WRITA), and precharge command (PRE).

### DATA INPUT AND OUTPUT ($DQ_0$ to $DQ_3$)

Input data is latched and written into the memory at the clock following the write command input. Data output is obtained by the following conditions followed by a read command input:

**$t_{RAC}$** ; from the bank active command when $t_{RCD}$ (min) is satisfied. (This parameter is reference only.)
**$t_{CAC}$** ; from the read command when $t_{RCD}$ is greater than $t_{RCD}$ (min). (This parameter is reference only.)
**$t_{AC}$** ; from the clock edge after $t_{RAC}$ and $t_{CAC}$.

The polarity of the output data is identical to that of the input. Data is valid between access time (determined by the three conditions above) and the next positive clock edge ($t_{OH}$).

### DATA I/O MASK (DQM)

DQM is an active high enable input and has an output disable and input mask function. During burst cycle and when DQM = High is latched by a clock, input is masked at the same clock and output will be masked at the second clock later while internal burst counter will increment by one or will go to the next stage depending on burst type.

### BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access. The burst mode is implemented by keeping the same Row address and by automatic strobing column address. Access time and cycle time of Burst mode is specified as $t_{AC}$ and $t_{CK}$, respectively. The internal column address counter operation is determined by a mode register which defines burst type and burst count length of 1, 2, 4 or 8 bits of boundary. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 1, the following combinations will be required:

| Current Stage | Next Stage | Method (Assert the following command) | |
|---|---|---|---|
| Burst Read | Burst Read | Read Command | |
| Burst Read | Burst Write | 1st Step | Mask Command (Normally 3 clock cycles) |
| | | 2nd Step | Write Command after $l_{OWD}$ |
| Burst Write | Burst Write | Write Command | |
| Burst Write | Burst Read | Read Command | |
| Burst Read | Precharge | Precharge Command | |
| Burst Write | Precharge | Precharge Command | |

The burst type can be selected either sequential or interleave mode if burst length is 2, 4 or 8. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least significant address (= 0). The interleave mode is a scrambled decoding scheme for $A_0$ and $A_2$. If the first access of column address is even (0), the next address will be odd (1), or vice-versa.

*(Continued)*

*(Continued)*

When the full burst operation is executed at single write mode, Auto-precharge command is valid only at write operation.

The burst type can be selected either sequential or interleave mode. But only the sequential mode is usable to the full column burst. The sequential mode is an incremental decoding scheme within a boundary address to be determined by burst length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least significant address (= 0).

| Burst Length | Starting Column Address $A_2$ $A_1$ $A_0$ | Sequential Mode | Interleave |
|---|---|---|---|
| 2 | X X 0 | 0 – 1 | 0 – 1 |
| | X X 1 | 1 – 0 | 1 – 0 |
| 4 | X 0 0 | 0 – 1 – 2 – 3 | 0 – 1 – 2 – 3 |
| | X 0 1 | 1 – 2 – 3 – 0 | 1 – 0 – 3 – 2 |
| | X 1 0 | 2 – 3 – 0 – 1 | 2 – 3 – 0 – 1 |
| | X 1 1 | 3 – 0 – 1 – 2 | 3 – 2 – 1 – 0 |
| 8 | 0 0 0 | 0 – 1 – 2 – 3 – 4 – 5 – 6 – 7 | 0 – 1 – 2 – 3 – 4 – 5 – 6 – 7 |
| | 0 0 1 | 1 – 2 – 3 – 4 – 5 – 6 – 7 – 0 | 1 – 0 – 3 – 2 – 5 – 4 – 7 – 6 |
| | 0 1 0 | 2 – 3 – 4 – 5 – 6 – 7 – 0 – 1 | 2 – 3 – 0 – 1 – 6 – 7 – 4 – 5 |
| | 0 1 1 | 3 – 4 – 5 – 6 – 7 – 0 – 1 – 2 | 3 – 2 – 1 – 0 – 7 – 6 – 5 – 4 |
| | 1 0 0 | 4 – 5 – 6 – 7 – 0 – 1 – 2 – 3 | 4 – 5 – 6 – 7 – 0 – 1 – 2 – 3 |
| | 1 0 1 | 5 – 6 – 7 – 0 – 1 – 2 – 3 – 4 | 5 – 4 – 7 – 6 – 1 – 0 – 3 – 2 |
| | 1 1 0 | 6 – 7 – 0 – 1 – 2 – 3 – 4 – 5 | 6 – 7 – 4 – 5 – 2 – 3 – 0 – 1 |
| | 1 1 1 | 7 – 0 – 1 – 2 – 3 – 4 – 5 – 6 | 7 – 6 – 5 – 4 – 3 – 2 – 1 – 0 |

## FULL COLUMN BURST AND BURST STOP COMMAND (BST)

The full column burst is an option of burst length and available only at sequential mode of burst type. This full column burst mode is repeatedly access to the same column. If burst mode reaches end of column address, then it wraps round to first column address (= 0) and continues to count until interrupted by the news read (READ) /write (WRIT), precharge (PRE), or burst stop (BST) command. The selection of Auto-precharge option is illegal during the full column burst operation except write command at BURST READ & SINGLE WRITE mode.

The BST command is applicable to terminate the burst operation. If the BST command is asserted during the burst mode, its operation is terminated immediately and the internal state moves to Bank Active.

When read mode is interrupted by BST command, the output will be in High-Z.
For the detail rule, please refer to Timing Diagram-8.
When write mode is interrupted by BST command, the data to be applied at the same time with BST command will be ignored.

## BURST READ & SINGLE WRITE

The burst read and single write mode provides single word write operation regardless of its burst length. In this mode, burst read operation does not be affected by this mode.

### PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

SDRAM memory core is the same as conventional DRAMs', requiring precharge and refresh operations. Precharge rewrites the bit line and to reset the internal Row address line and is executed by the Precharge command (PRE). With the Precharge command, SDRAM will automatically be in standby state after precharge time ($t_{RP}$).

The precharged bank is selected by combination of AP and $A_{13}$, $A_{12}$ when Precharge command is asserted. If AP = High, all banks are precharged regardless of $A_{13}$, $A_{12}$ (PALL). If AP = Low, a bank to be selected by $A_{13}$, $A_{12}$ is precharged (PRE).
The auto-precharge enters precharge mode at the end of burst mode of read or write without Precharge command assertion.
This auto precharge is entered by AP = High when a read or write command is asserted. Refer to FUNCTIONAL TRUTH TABLE.

### AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The SDRAM Auto-refresh command (REF) generates Precharge command internally. All banks of SDRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be asserted every 16 µs or a total 4096 refresh commands within a 65.6 ms period.

### SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh function until cancelled by SELFX.

The Self-refresh is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF). Once SDRAM enters the self-refresh mode, all inputs except for CKE will be "don't care" (either logic high or low level state) and outputs will be in a High-Z state. During a self-refresh mode, CKE = Low should be maintained. SELF command should only be issued after last read data has been appeared on DQ.

**Note:** When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted prior to the self-refresh mode entry.

### SELF-REFRESH EXIT (SELFX)

To exit self-refresh mode, apply minimum $t_{PDE}$ after CKE brought high, and then the NOP command (NOP) or the Deselect command (DESL) should be asserted within one $t_{RC}$ period. CKE should be held High within one $t_{RC}$ period after $t_{PDE}$. Refer to Timing Diagram for the detail.

It is recommended to assert an Auto-refresh command just after the $t_{RC}$ period to avoid the violation of refresh period.

**Note:** When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted after the self-refresh exit.

### MODE REGISTER SET (MRS)

The mode register of SDRAM provides a variety of different operations. The register consists of four operation fields; Burst Length, Burst Type, CAS latency, and Operation Code. Refer to MODE REGISTER TABLE in page 33.

The mode register can be programmed by the Mode Register Set command (MRS). Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command (or part loses power). MRS command should only be issued on condition that all DQ is in Hi-Z.

The condition of the mode register is undefined after the power-up stage. It is required to set each field after initialization of SDRAM. Refer to POWER-UP INITIALIZATION below.

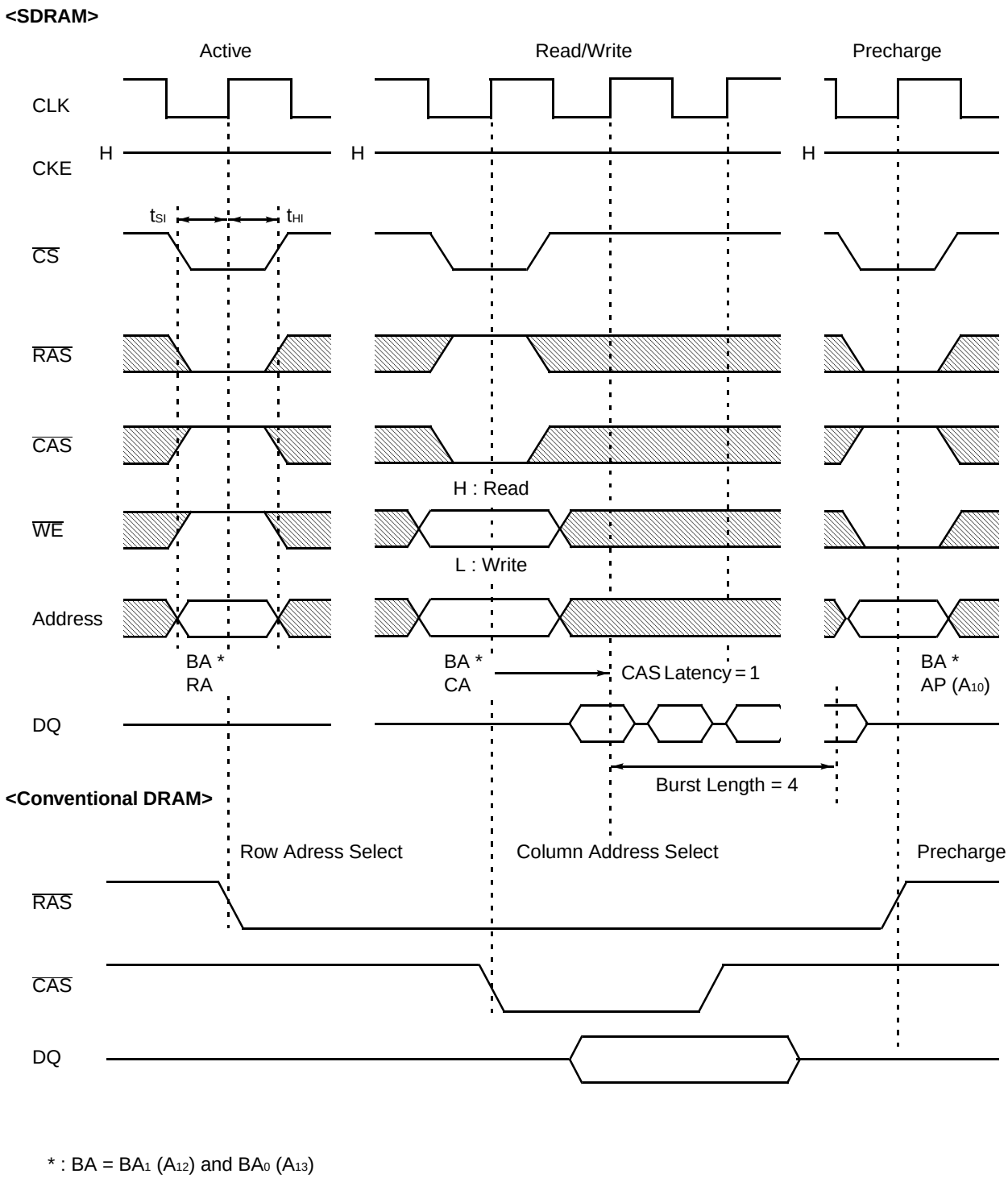
## POWER-UP INITIALIZATION

The SDRAM internal condition after power-up will be undefined. It is required to follow the following Power On Sequence to execute read or write operation.

1. Apply power and start clock. Attempt to maintain either NOP or DESL command at the input.
2. Maintain stable power, stable clock, and NOP condition for a minimum of 200 μs.
3. Precharge all banks by Precharge (PRE) or Precharge All command (PALL).
4. Assert minimum of 8 Auto-refresh command (REF).
5. Program the mode register by Mode Register Set command (MRS).

In addition, it is recommended DQM and CKE to track $V_{CC}$ to insure that output is High-Z state. The Mode Register Set command (MRS) can be set before 8 Auto-refresh command (REF).

**Fig. 2 – BASIC TIMING FOR CONVENTIONAL DRAM VS SYNCHRONOUS DYNAMIC RAM**




* : BA = $BA_1$ ($A_{12}$) and $BA_0$ ($A_{13}$)

## MINIMUM CLOCK LATENCY OR DELAY TIME FOR 1 BANK OPERATION

| First command \ Second command (same bank) | MRS | ACTV | READ | READA | WRIT | WRITA | PRE | PALL | REF | SELF |
|---|---|---|---|---|---|---|---|---|---|---|
| **MRS** | $t_{RSC}$ | $t_{RSC}$ | | | | | $t_{RSC}$ | $t_{RSC}$ | $t_{RSC}$ | $t_{RSC}$ |
| **ACTV** | | | $t_{RCD}$ | $t_{RCD}$ *4 | $t_{RCD}$ | $t_{RCD}$ *4 | $t_{RAS}$ | $t_{RAS}$ | | |
| **READ** | | | 1 | 1 | 4 *1 | 4 *1 | 1 | 1 | | |
| **READA** | BL + $t_{RP}$ *2 | BL + $t_{RP}$ *2 | | | | | | | BL + $t_{RP}$ *2 | BL + $t_{RP}$ *2 |
| **WRIT** | | | $t_{WR}$ | $t_{WR}$ | 1 | 1 | $t_{DPL}$ | $t_{DPL}$ | | |
| **WRITA** | $t_{DAL}$ | $t_{DAL}$ | | | | | | | $t_{DAL}$ | $t_{DAL}$ |
| **PRE** | $t_{RP}$ *3 | $t_{RP}$ *3 | | | | | $t_{RP}$ | $t_{RP}$ | $t_{RP}$ *3 | $t_{RP}$ *3 |
| **PALL** | $t_{RP}$ *3 | $t_{RP}$ *3 | | | | | $t_{RP}$ | $t_{RP}$ | $t_{RP}$ *3 | $t_{RP}$ *3 |
| **REF** | $t_{RC}$ | $t_{RC}$ | | | | | $t_{RC}$ | $t_{RC}$ | $t_{RC}$ | $t_{RC}$ |
| **SELFX** | $t_{RC}$ | $t_{RC}$ | | | | | | | $t_{RC}$ | $t_{RC}$ |

**Notes:** *1. Assume no I/O conflict.
*2. If $t_{RP} \leq t_{CK}$, minimum latency is a sum of BL + CL.
*3. Assume output is in High-Z state.
*4. Assume $t_{RAS}$ is satisfied.

Illegal Command

# MB81F64442B-103E/-103/-10/-103L/-10L

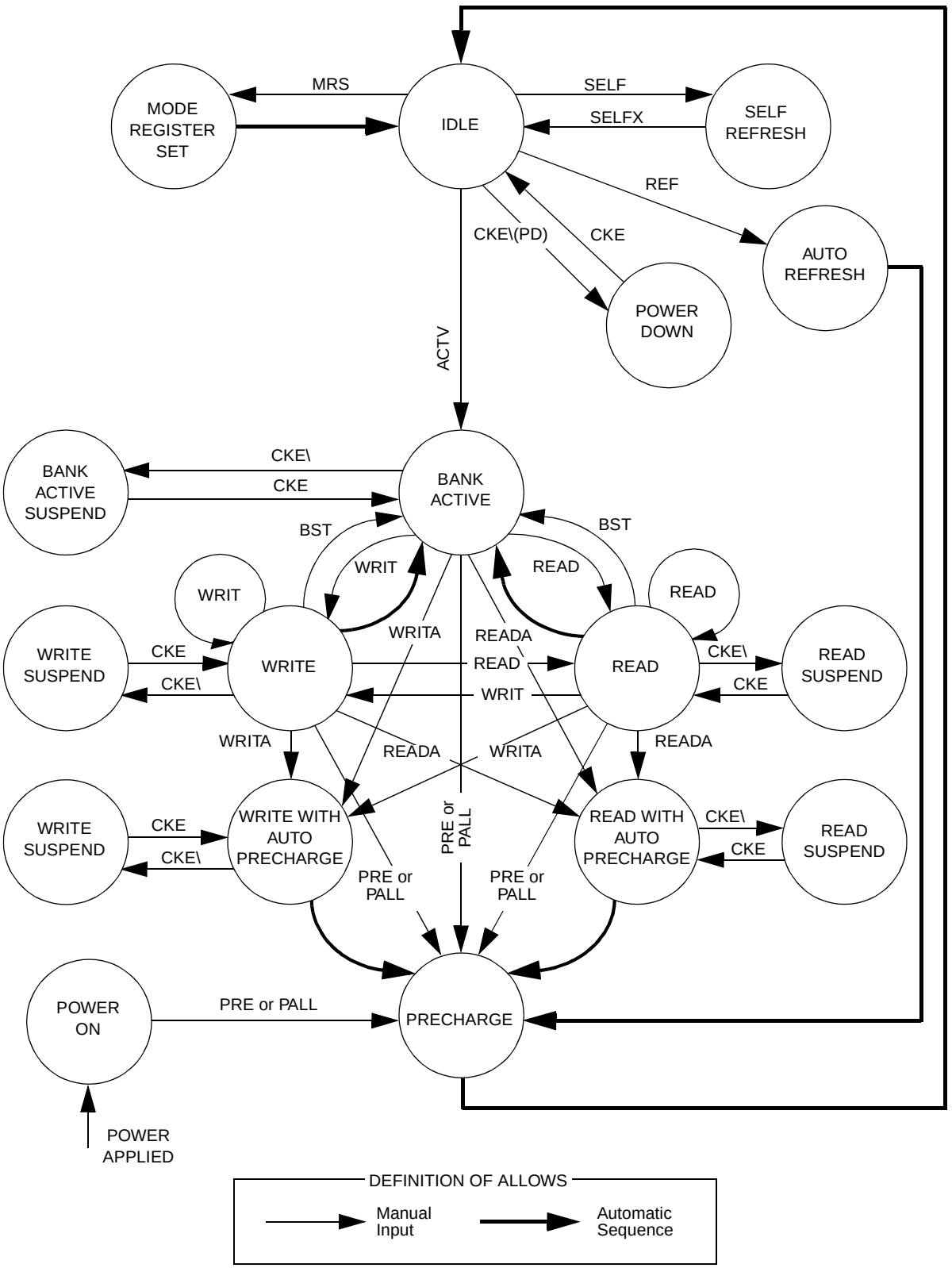
## MINIMUM CLOCK LATENCY OR DELAY TIME FOR MULTI BANK OPERATION

| First command \ Second command (other bank) | MRS | ACTV | READ | READA | WRIT | WRITA | PRE | PALL | REF | SELF |
|---|---|---|---|---|---|---|---|---|---|---|
| **MRS** | $t_{RSC}$ | $t_{RSC}$ | | | | | $t_{RSC}$ | $t_{RSC}$ | $t_{RSC}$ | $t_{RSC}$ |
| **ACTV** | | *1 $t_{RRD}$ | *2 1 | *2 1 | *2 1 | *2 1 | *7 1 | *2 $t_{RAS}$ | | |
| **READ** | | *1 1 | *2 1 | *2 1 | *2 *3 4 | *2 *3 4 | *7 1 | *8 1 | | |
| *9 **READA** | *1 *4 BL+ $t_{RP}$ | *1 1 | *2 1 | *2 1 | *2 *3 4 | *2 *3 4 | 1 | | *1 *4 BL+ $t_{RP}$ | *1 *4 BL+ $t_{RP}$ |
| **WRIT** | | *1 1 | *2 1 | *2 1 | *2 1 | *2 1 | *7 1 | *8 1 | | |
| *9 **WRITA** | *1 *4 BL+ $t_{RP}$ | *1 1 | *2 1 | *2 1 | *2 1 | *2 1 | 1 | | *1 BL+ $t_{RP}$ | *1 BL+ $t_{RP}$ |
| **PRE** | *1 $t_{RP}$ | *1 1 | *2 1 | *2 1 | *2 1 | *2 1 | 1 | *2 $t_{RAS}$ | *1 $t_{RP}$ | *1 $t_{RP}$ |
| *5 **PALL** | $t_{RP}$ | $t_{RP}$ | | | | | 1 | 1 | *1 *6 $t_{RP}$ | *1 *6 $t_{RP}$ |
| **REF** | $t_{RC}$ | $t_{RC}$ | | | | | $t_{RC}$ | $t_{RC}$ | $t_{RC}$ | $t_{RC}$ |
| **SELFX** | $t_{RC}$ | $t_{RC}$ | | | | | | | $t_{RC}$ | $t_{RC}$ |

**Notes:** *1. Assume other banks is in idle state.
*2. Assume other banks is in active state.
*3. Assume no I/O conflict.
*4. If $t_{RP} \leq t_{CK}$, minimum latency is a sum of BL + CL.
*5. Assume PALL command dose not affect any operation on other banks.
*6. Assume output is in High-Z sate.
*7. Assume $t_{RAS}$ of other banks is satisfied.
*8. Assume $t_{RAS}$ (ACTV to PALL) is satisfied.
*9. If other banks should be interrupted, $t_{RAS}$ of own bank is satisfied.


Illegal Command

**Fig. 3 – STATE DIAGRAM (Simplified for Single BANK Operation State Diagram)**



## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage of $V_{CC}$ Supply Relative to $V_{SS}$ | $V_{CC}$, $V_{CCQ}$ | –0.5 to +4.6 | V |
| Voltage at Any Pin Relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | –0.5 to +4.6 | V |
| Short Circuit Output Current | $I_{OUT}$ | –50 to +50 | mA |
| Power Dissipation | $P_D$ | 1.0 | W |
| Storage Temperature | $T_{STG}$ | –55 to +125 | °C |

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

**(Referenced to $V_{SS}$)**

| Parameter | Notes | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$, $V_{CCQ}$ | 3.0 | 3.3 | 3.6 | V |
| | | $V_{SS}$, $V_{SSQ}$ | 0 | 0 | 0 | V |
| Input High Voltage | *1 | $V_{IH}$ | 2.0 | — | $V_{CC}$ + 0.5 | V |
| Input Low Voltage | *2 | $V_{IL}$ | –0.5 | — | 0.8 | V |
| Ambient Temperature | | $T_A$ | 0 | — | 70 | °C |

**Notes:** *1. Overshoot limit: $V_{IH}$ (max) = $V_{CC}$ +1.5 V with a pulsewidth ≤ 5 ns.
*2. Undershoot limit: $V_{IL}$ (min) = –1.5 V with a pulsewidth ≤ 5 ns.

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

## ■ CAPACITANCE

($T_A$ = 25°C, f = 1 MHz)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Capacitance, Except for CLK | $C_{IN1}$ | 2.5 | — | 5.0 | pF |
| Input Capacitance for CLK | $C_{IN2}$ | 2.5 | — | 4.0 | pF |
| I/O Capacitance | $C_{I/O}$ | 4.0 | — | 6.5 | pF |

## ■ DC CHARACTERISTICS

**(At recommended operating conditions unless otherwise noted.) Notes 1, 2**

| Parameter | | Symbol | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Output High Voltage | | $V_{OH(DC)}$ | $I_{OH}$ = –2 mA | 2.4 | — | V |
| Output Low Voltage | | $V_{OL(DC)}$ | $I_{OL}$ = 2 mA | — | 0.4 | V |
| Input Leakage Current (Any Input) | | $I_{LI}$ | 0 V ≤ $V_{IN}$ ≤ $V_{CC}$; All other pins not under test = 0 V | –10 | 10 | µA |
| Output Leakage Current | | $I_{LO}$ | 0 V ≤ $V_{IN}$ ≤ $V_{CC}$; Data out disabled | –10 | 10 | µA |
| Operating Current (Average Power Supply Current) | MB81F64442B -103E/-103/103L | $I_{CC1S}$ | Burst: Length = 4<br>$t_{RC}$ = min for BL = 4<br>$t_{CK}$ = min<br>One bank active<br>Outputs open<br>Addresses changed up to 3-times during $t_{RC}$ (min)<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 120 | mA |
| | MB81F64442B -10/10L | | | | 100 | |
| | MB81F64442B -103E/-103/103L | $I_{CC1D}$ | Burst: Length = 4<br>(each Bank)<br>$t_{RC}$ = min for BL = 4<br>(each Bank)<br>$t_{CK}$ = min<br>2 banks active<br>Outputs open<br>Addresses changed up to 3-times during $t_{RC}$ (min)<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 220 | mA |
| | MB81F64442B -10/10L | | | | 180 | |
| Precharge Standby Current (Power Supply Current) | MB81F64442B -103E | $I_{CC2P}$ | CKE = $V_{IL}$<br>All banks idle<br>$t_{CK}$ = min<br>Power down mode<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 3 | mA |
| | MB81F64442B -103/10 | | | — | 2 | |
| | MB81F64442 -103L/10L | | | — | 1 | |
| | MB81F64442B -103E/-103/10 | $I_{CC2PS}$ | CKE = $V_{IL}$<br>All banks idle<br>CLK = H or L<br>Power down mode<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 2 | mA |
| | MB81F64442 -103L/10L | | | — | 0.5 | |
| | | $I_{CC2N}$ | CKE = $V_{IH}$<br>All banks idle, $t_{CK}$ = min<br>NOP commands only,<br>Input signals (except to CMD) are changed one time during 3 clock cycles<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 20 | mA |
| | | $I_{CC2NS}$ | CKE = $V_{IH}$<br>All banks idle<br>CLK = H or L<br>Input signal are stable<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 5 | mA |

*(Continued)*

*(Continued)*

| Parameter | | Symbol | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Active Standby Current (Power Supply Current) | MB81F64442B -103E/-103/10 | $I_{CC3P}$ | CKE = $V_{IL}$<br>Any bank active<br>$t_{CK}$ = min<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 5 | mA |
| | MB81F64442B -103L/10L | | | — | 3 | |
| | MB81F64442B -103E/-103/10 | $I_{CC3PS}$ | CKE = $V_{IL}$<br>Any bank active<br>CLK = H or L<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 4 | mA |
| | MB81F64442B -103L/10L | | | — | 2 | |
| | | $I_{CC3N}$ | CKE = $V_{IH}$<br>Any bank active<br>$t_{CK}$ = min<br>NOP commands only,<br>Input signals (except to CMD) are changed one time during 3 clock cycles<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 30 | mA |
| | | $I_{CC3NS}$ | CKE = $V_{IH}$<br>Any bank active<br>CLK = H or L<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 10 | mA |
| Burst mode Current (Average Power Supply Current) | | $I_{CC4}$ | $t_{CK}$ = min<br>Burst Length = 4<br>Outputs open<br>Multiple-banks active<br>Gapless data<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 140 | mA |
| Refresh Current #1 (Average Power Supply Current) | MB81F64442B -103E/-103/103L | $I_{CC5}$ | Auto-refresh;<br>$t_{CK}$ = min<br>$t_{RC}$ = min<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 200 | mA |
| | MB81F64442B -10/10L | | | — | 180 | |
| Refresh Current #2 (Average Power Supply Current) | MB81F64442B -103E | $I_{CC6}$ | Self-refresh;<br>$t_{CK}$ = min<br>CKE ≤ 0.2 V<br>0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 2 | mA |
| | MB81F64442B -103/10 | | | — | 1 | |
| | MB81F64442B -103L/10L | | | — | 0.5 | |

## ■ AC CHARACTERISTICS

**(At recommended operating conditions unless otherwise noted.) Note 2, 3, 4**

| Parameter | Notes | | Symbol | MB81F64442B-103E/-103/-103L | | MB81F64442B-10/-10L | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| Clock Period | | CL = 2 | $t_{CK2}$ | 15 | — | 15 | — | ns |
| | | CL = 3 | $t_{CK3}$ | 10 | | 10 | | ns |
| Clock High Time | | | $t_{CH}$ | 3 | — | 3 | — | ns |
| Clock Low Time | | | $t_{CL}$ | 3 | — | 3 | — | ns |
| Input Setup Time | | | $t_{SI}$ | 2 | — | 2 | — | ns |
| Input Hold Time | | | $t_{HI}$ | 1 | — | 1 | — | ns |
| Access Time from Clock ($t_{CK}$ = min) | *5, 6 | CL = 2 | $t_{AC2}$ | — | 8 | — | 8 | ns |
| | | CL = 3 | $t_{AC3}$ | | 6 | | 6 | ns |
| Output in Low-Z | *7 | | $t_{LZ}$ | 0 | — | 0 | — | ns |
| Output in High-Z | *7 | CL = 2 | $t_{HZ2}$ | 3 | 8 | 3 | 8 | ns |
| | | CL = 3 | $t_{HZ3}$ | | 6 | | 6 | ns |
| Output Hold Time | *7 | | $t_{OH}$ | 3 | — | 3 | — | ns |
| Time between Refresh | | | $t_{REF}$ | — | 65.6 | — | 65.6 | ms |
| Transition Time | | | $t_T$ | 0.5 | 2 | 0.5 | 2 | ns |
| CKE Setup Time for Power Down Exit Time | | | $t_{CKSP}$ | 3 | — | 3 | — | ns |

## BASE VALUES FOR CLOCK COUNT/LATENCY

| Parameter | Notes | | Symbol | MB81F64442B-103E/-103/-103L | | MB81F64442B-10/-10L | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| $\overline{RAS}$ Cycle Time | *8 | | $t_{RC}$ | 70 | — | 80 | — | ns |
| $\overline{RAS}$ Precharge Time | | | $t_{RP}$ | 20 | — | 30 | — | ns |
| $\overline{RAS}$ Active Time | | | $t_{RAS}$ | 50 | 110000 | 50 | 110000 | ns |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | *9 | | $t_{RCD}$ | 20 | — | 30 | — | ns |
| Write Recovery Time | | | $t_{WR}$ | 10 | — | 10 | — | ns |
| $\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time | | | $t_{RRD}$ | 20 | — | 20 | — | ns |
| Data-in to Precharge Lead Time | | | $t_{DPL}$ | 10 | — | 10 | — | ns |
| Data-in to Active/Refresh Command Period | | CL=2 | $t_{DAL2}$ | 1 cyc + $t_{RP}$ | — | 1 cyc + $t_{RP}$ | — | ns |
| | | CL=3 | $t_{DAL3}$ | 2 cyc + $t_{RP}$ | — | 2 cyc + $t_{RP}$ | — | ns |
| Mode Resister Set Cycle Time | | | $t_{RSC}$ | 20 | — | 20 | — | ns |

## CLOCK COUNT FORMULA Note 13

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad \text{(Round off a whole number)}$$

## LATENCY - FIXED VALUES

**(The latency values on these parameters are fixed regardless of clock period.)**

| Parameter | Notes | Symbol | MB81F64442B-103E/-103/-103L | MB81F64442B-10/-10L | Unit |
|---|---|---|---|---|---|
| CKE to Clock Disable | | $l_{CKE}$ | 1 | 1 | cycle |
| DQM to Output in High-Z | | $l_{DQZ}$ | 2 | 2 | cycle |
| DQM to Input Data Delay | | $l_{DQD}$ | 0 | 0 | cycle |
| Last Output to Write Command Delay | | $l_{OWD}$ | 2 | 2 | cycle |
| Write Command to Input Data Delay | | $l_{DWD}$ | 0 | 0 | cycle |
| Precharge to Output in High-Z Delay | CL = 2 | $l_{ROH2}$ | 2 | 2 | cycle |
| | CL = 3 | $l_{ROH3}$ | 3 | 3 | cycle |
| Burst Stop Command to Output in High-Z Delay | CL = 2 | $l_{BSH2}$ | 2 | 2 | cycle |
| | CL = 3 | $l_{BSH3}$ | 3 | 3 | cycle |
| $\overline{CAS}$ to $\overline{CAS}$ Delay (min) | | $l_{CCD}$ | 1 | 1 | cycle |
| $\overline{CAS}$ Bank Delay (min) | | $l_{CBD}$ | 1 | 1 | cycle |

**Notes:** *1. $I_{CC}$ depends on the output termination or load conditions, clock cycle rate, signal clocking rate; the specified values are obtained with the output open and no termination register.

*2. An initial pause (DESL or NOP) of 200 µs is required after power-up followed by a minimum of eight Auto-refresh cycles.

*3. AC characteristics assume $t_T$ = 1 ns and 50 pF of capacitive load.

*4. 1.4 V is the reference level for measuring timing of input signals. Transition times are measured between $V_{IH}$ (min) and $V_{IL}$ (max). (See Fig. 5)

*5. Maximum value of CL = 2 depends on $t_{CK}$.

*6. $t_{AC}$ also specifies the access time at burst mode except for first access.

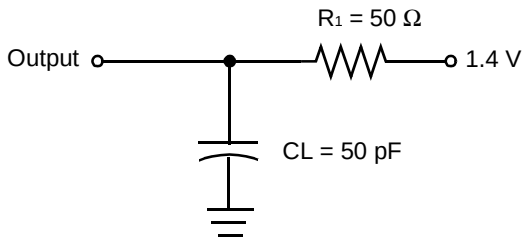
*7. Specified where output buffer is no longer driven. $t_{OH}$, $t_{LZ}$, and $t_{HZ}$ define the times at which the output level achieves ±200 mV.

*8. Actual clock count of $t_{RC}$ ($l_{RC}$) will be sum of clock count of $t_{RAS}$ ($l_{RAS}$) and $t_{RP}$ ($l_{RP}$).

*9. Operation within the $t_{RCD}$ (min) ensures that access time is detetermined by $t_{RCD}$ (min) + $t_{AC}$ (max); If $t_{RCD}$ is greater than the specified $t_{RCD}$ (min), access time is determined by $t_{AC}$.

*10. All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by a simple formula: clock count equals base value divided by clock period (round off to a whole number).

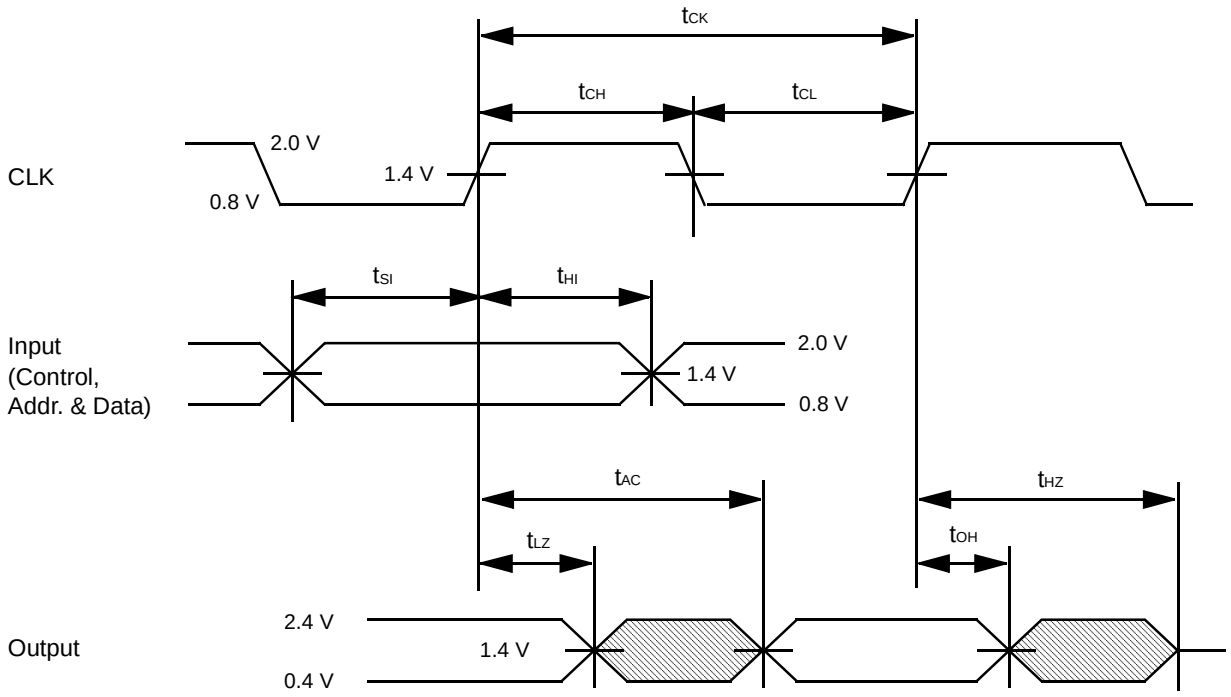
**Fig. 4 – EXAMPLE OF AC TEST LOAD CIRCUIT**




**LVTTL**

**Note:** AC characteristics are measured in this condition. This load circuits are not applicable for $V_{OH}$ and $V_{OL}$.

**Fig. 5 – TIMING DIAGRAM, SETUP, HOLD AND DELAY TIME**




**Note:** Reference level of input signal is 1.4 V for LVTTL.
Access time is measured at 1.4 V for LVTTL.

**Fig. 6 – TIMING DIAGRAM, DELAY TIME FOR POWER DOWN EXIT**

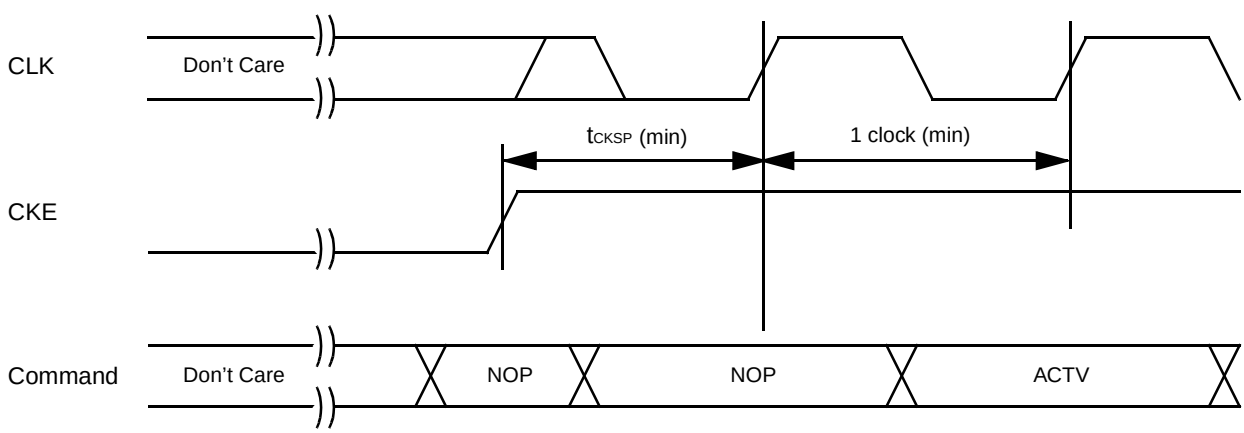
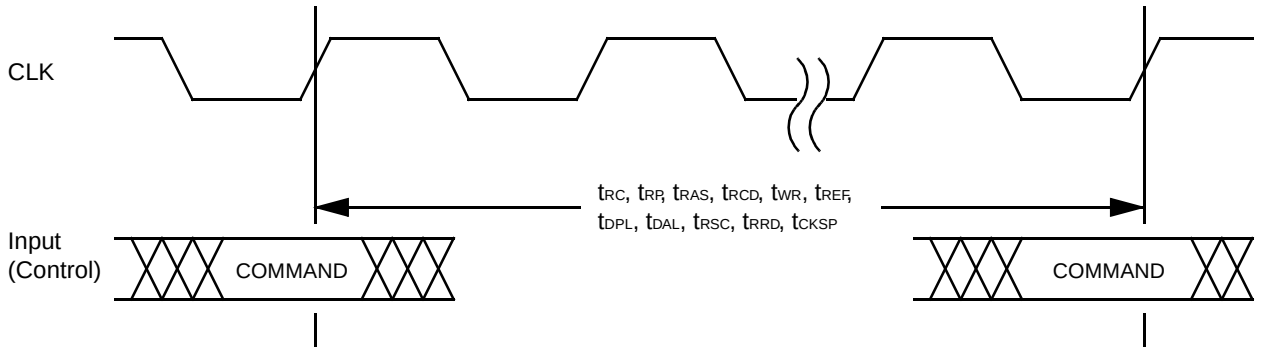
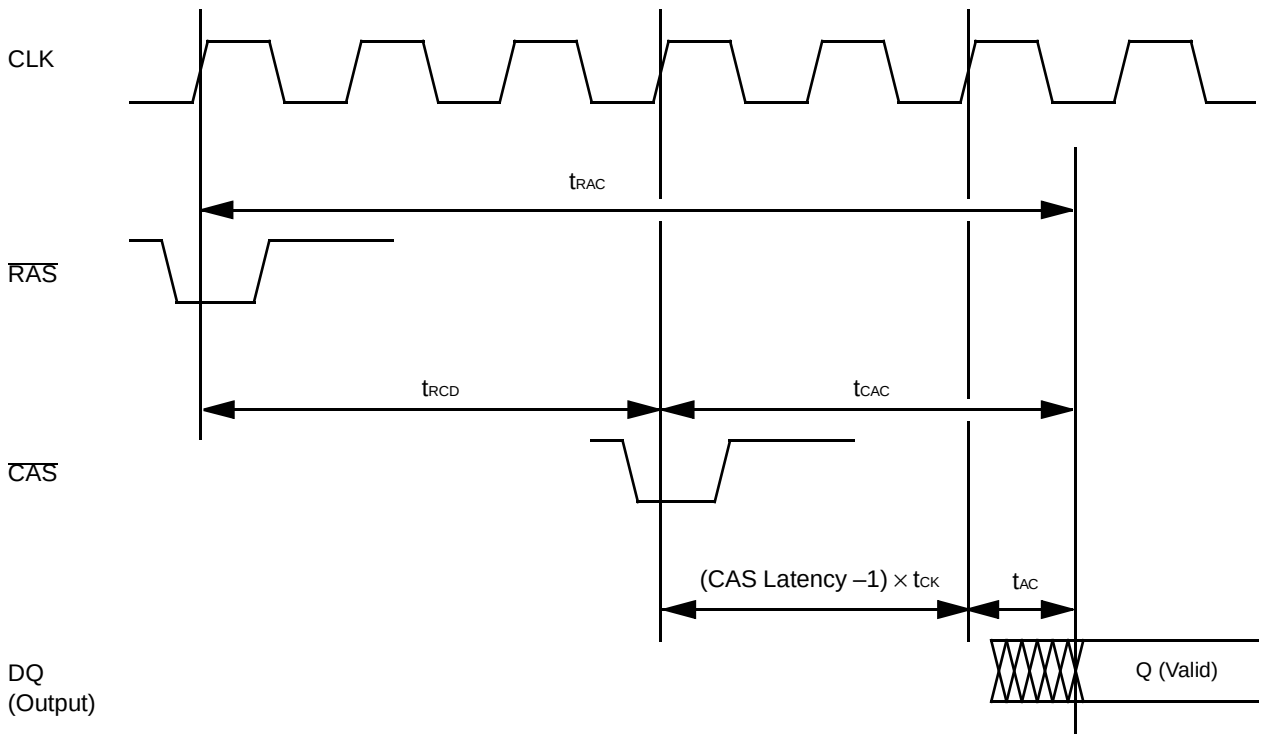


**Fig. 7 – TIMING DIAGRAM, PULSE WIDTH**




**Note:** This parameter is a limit value of the rising edge of the clock from one command input to next input. $t_{PDE}$ is the latency value from the rising edge of CKE.
Measurement reference voltage is 1.4 V.

**Fig. 8 – TIMING DIAGRAM, ACCESS TIME**




**Note:** $t_{RAC}$ and $t_{CAC}$ are reference values. Data can be obtained after both $t_{CAC}$ = (CL-1) × $t_{CK}$ and $t_{AC}$ is satisfied.

## ■ MODE REGISTER TABLE

### MODE REGISTER SET

| $A_{13}$ | $A_{12}$ | $A_{11}$ | $A_{10}$ | $A_9$ | $A_8$ | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | Op-code | 0 | 0 | CL | | | BT | BL | | | MODE REGISTER |

| $A_6$ | $A_5$ | $A_4$ | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

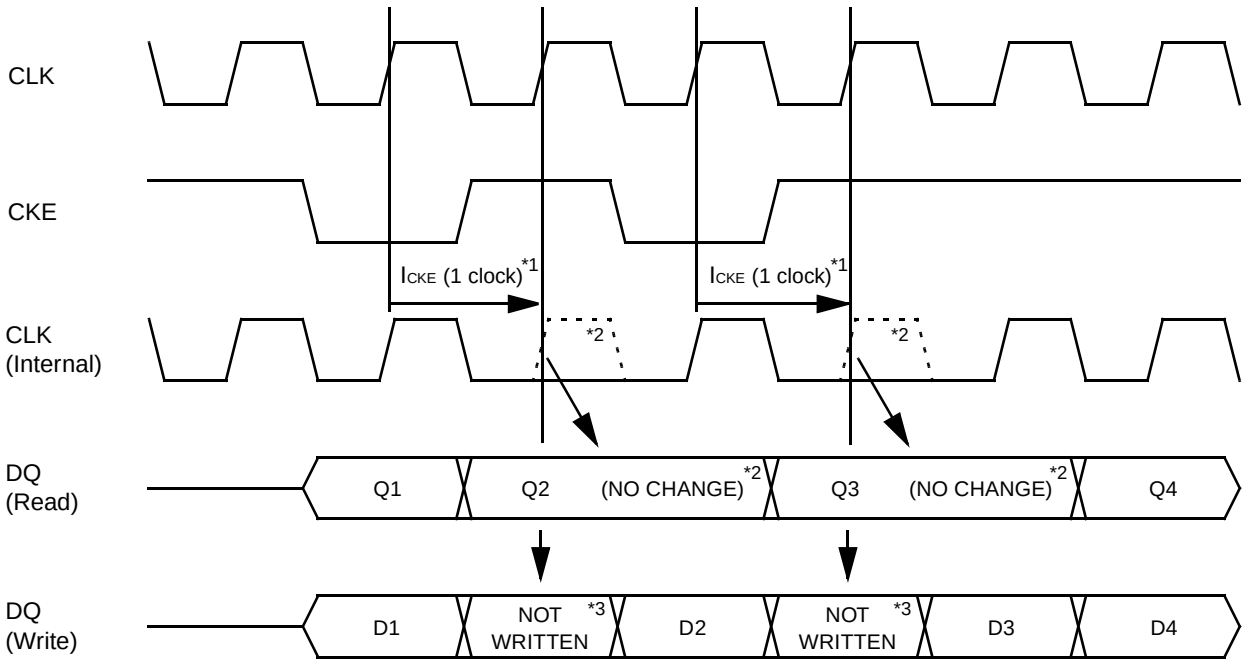
| $A_2$ | $A_1$ | $A_0$ | Burst Length | |
|---|---|---|---|---|
| | | | BT = 0 | BT = 1 |
| 0 | 0 | 0 | 1 | Reserved |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | Reserved | Reserved |
| 1 | 1 | 0 | Reserved | Reserved |
| 1 | 1 | 1 | Full Column | Reserved |

| $A_9$ | Op-code |
|---|---|
| 0 | Burst Read & Burst Write |
| 1 | Burst Read & Single Write |

| $A_3$ | Burst Type |
|---|---|
| 0 | Sequential (Wrap round, Binary-up) |
| 1 | Interleave (Wrap round, Binary-up) |

**Notes:** 1. When $A_9$ = 1, burst length at Write is always one regardless of BL value.
2. BL = 1 and Full Column are not applicable to the interleave mode.

## TIMING DIAGRAM – 1 : CLOCK ENABLE - READ AND WRITE SUSPEND (@ BL = 4)

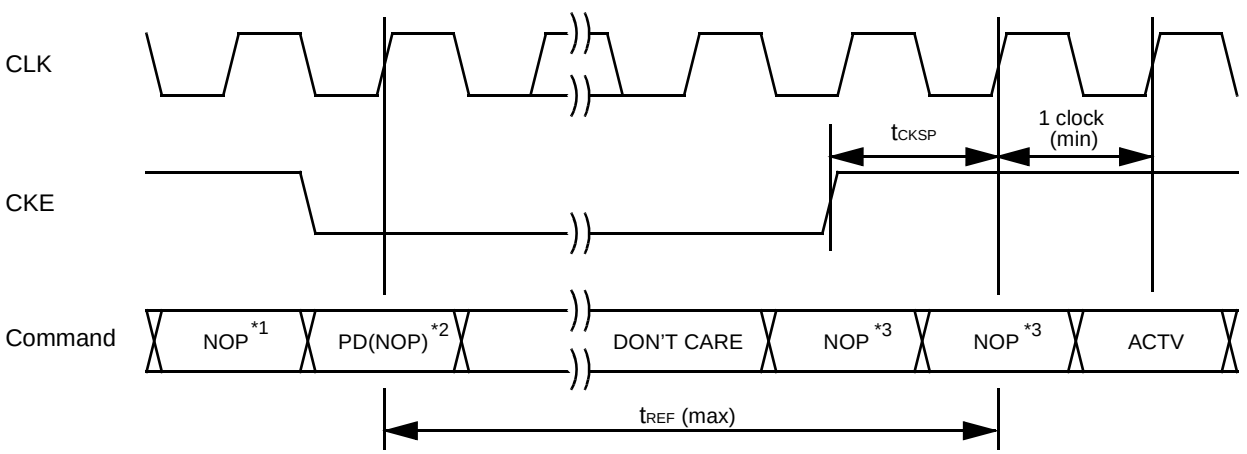



**Notes:** *1. The latency of CKE ($t_{CKE}$) is one clock.

*2. During read mode, burst counter will not be incremented/decremented at the next clock of CSUS command. Output remain the same data.

*3. During the write mode, data at the next clock of CSUS command is ignored.

## TIMING DIAGRAM – 2 : CLOCK ENABLE - POWER DOWN ENTRY AND EXIT

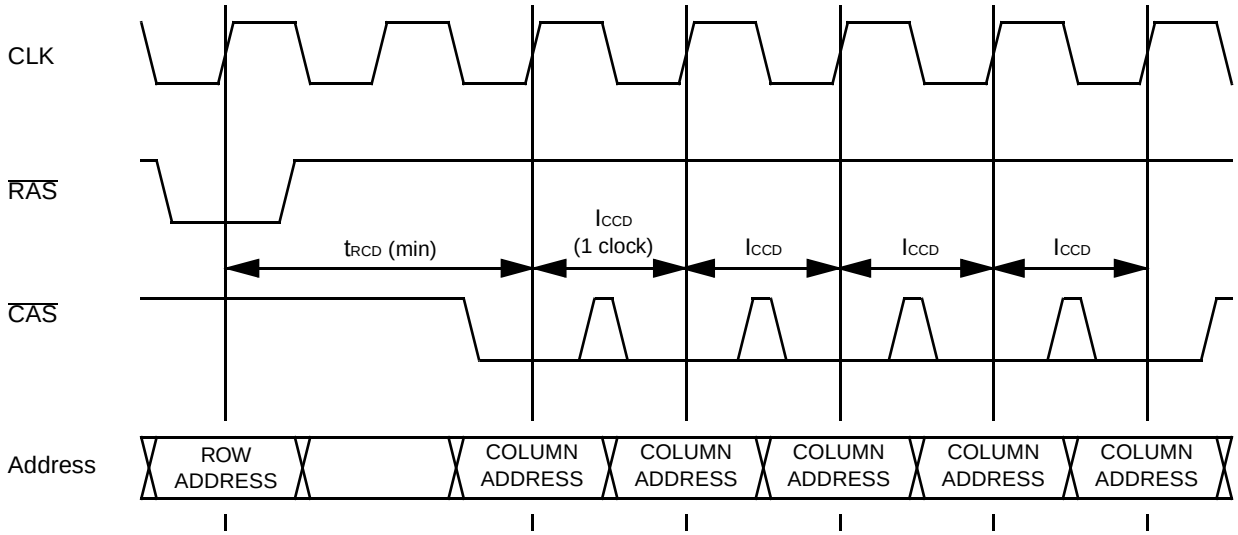



**Notes:** *1. Precharge command (PRE or PALL) should be asserted if any bank is active and in the burst mode.

*2. Precharge command can be posted in conjunction with CKE after the last read data have been appeared on DQ.

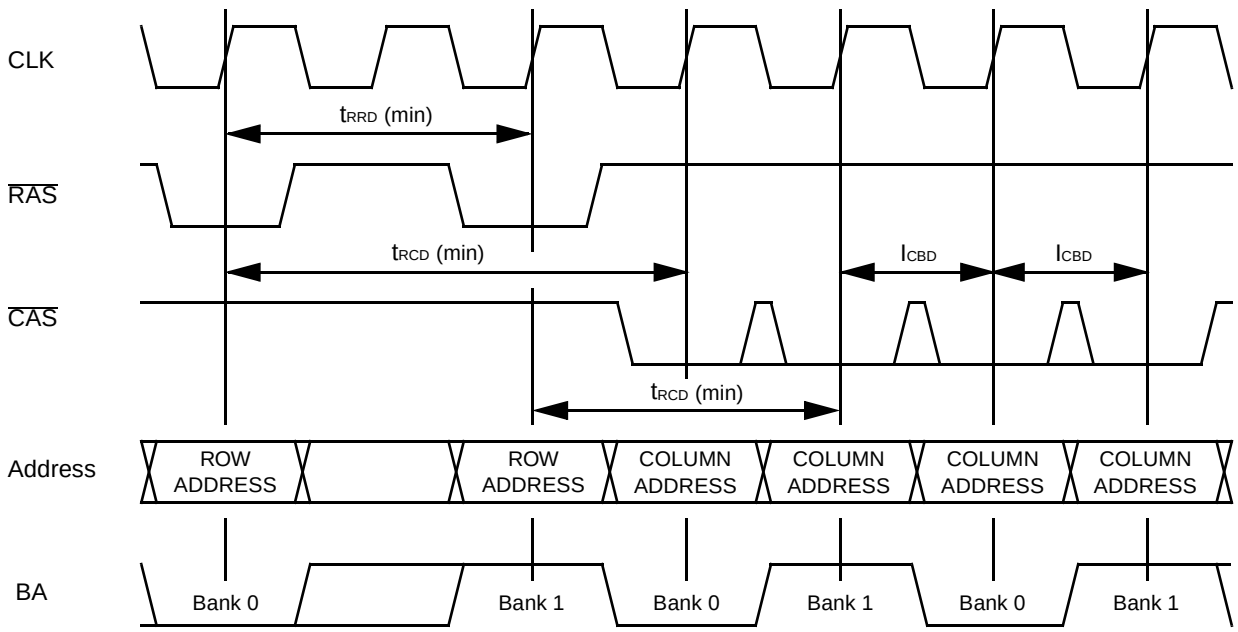
*3. The ACTV command can be latched after $t_{CKSP}$ (min) + 1 clock (min). It is recommended to apply NOP command in conjunction with CKE.

## TIMING DIAGRAM – 3 : COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY

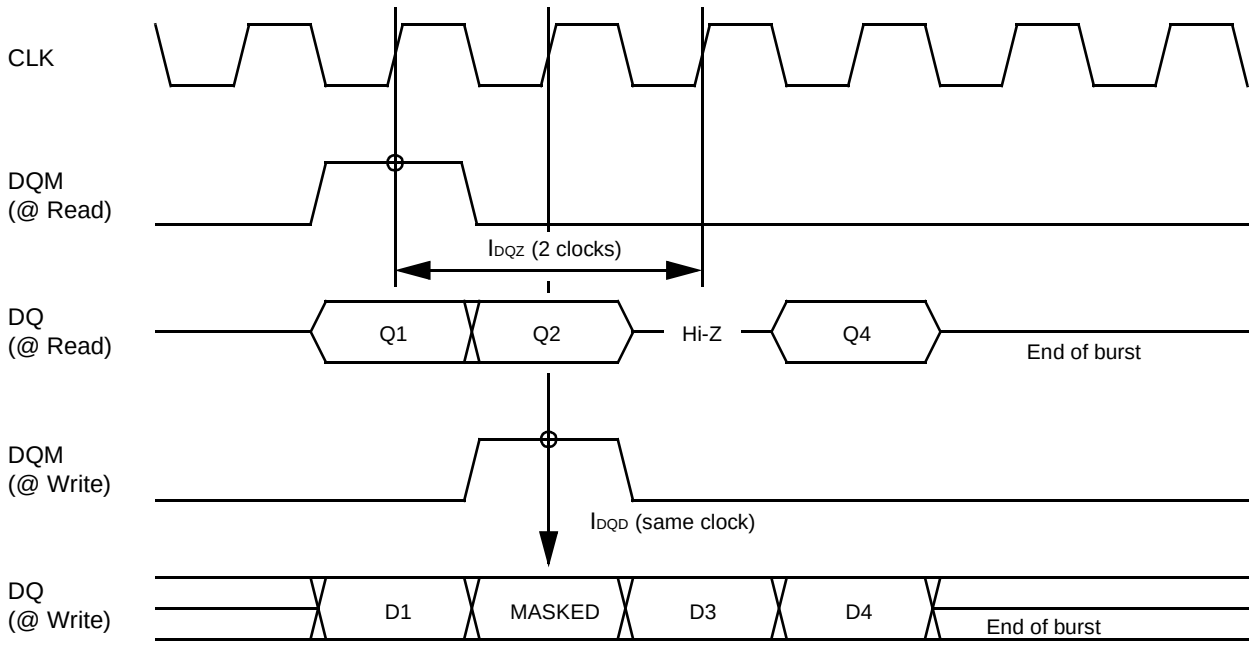



**Note:** $\overline{CAS}$ to $\overline{CAS}$ address delay can be one or more clock period.

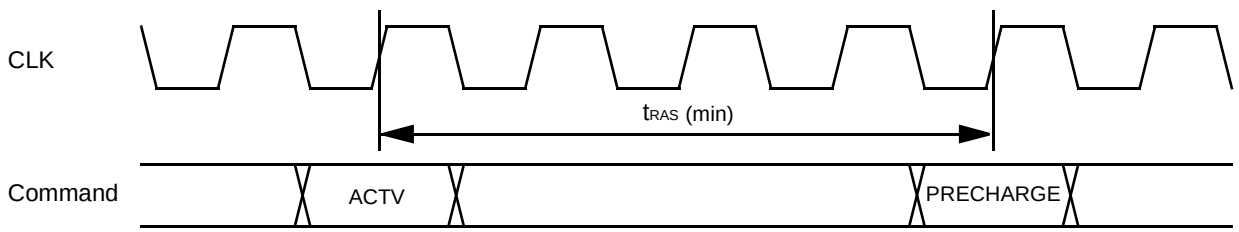
## TIMING DIAGRAM – 4 : DIFFERENT BANK ADDRESS INPUT DELAY



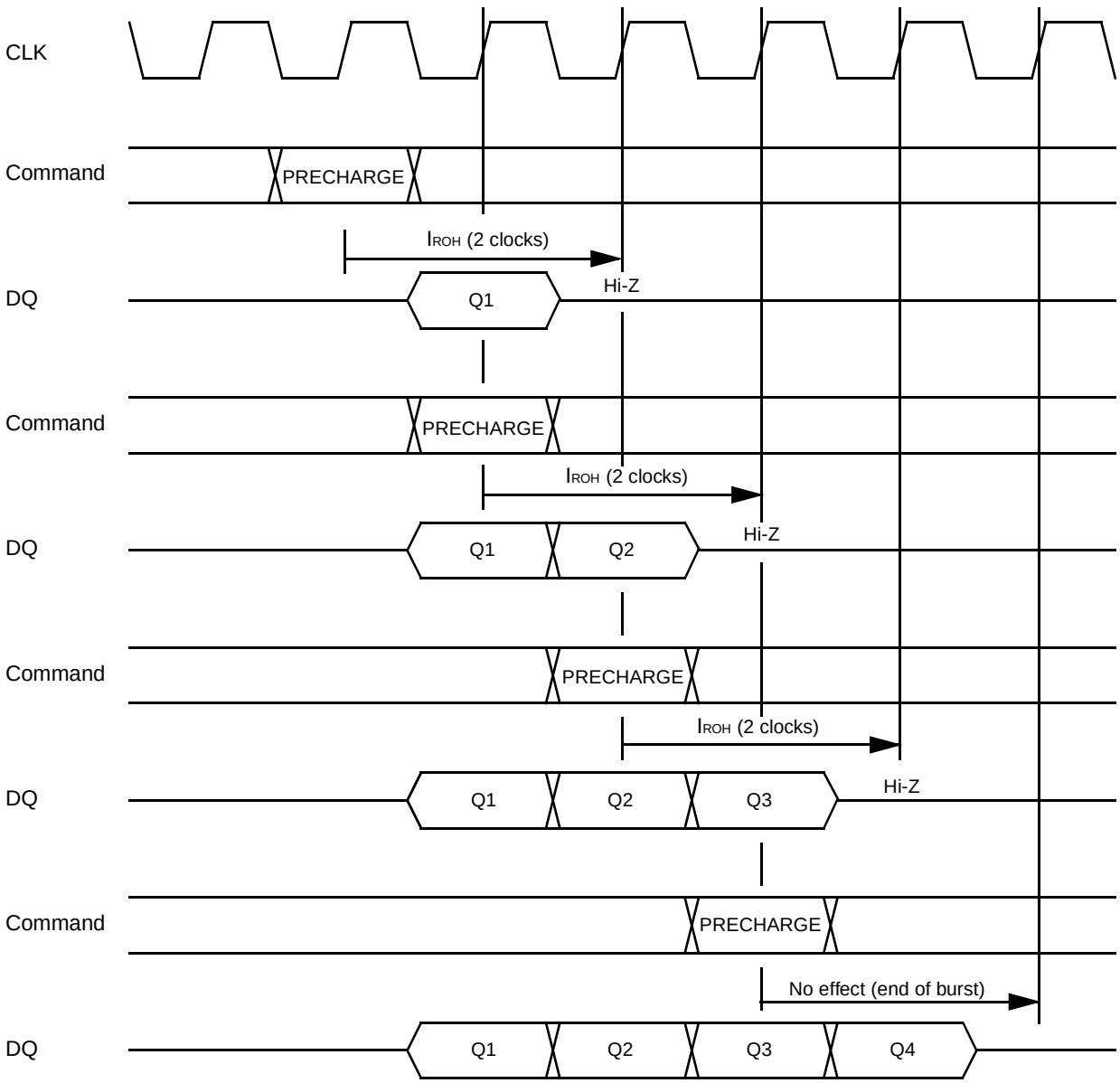
## TIMING DIAGRAM – 5 : DQM - INPUT MASK AND OUTPUT DISABLE (@ BL = 4)




## TIMING DIAGRAM – 6 : PRECHARGE TIMING (APPLIED TO THE SAME BANK)

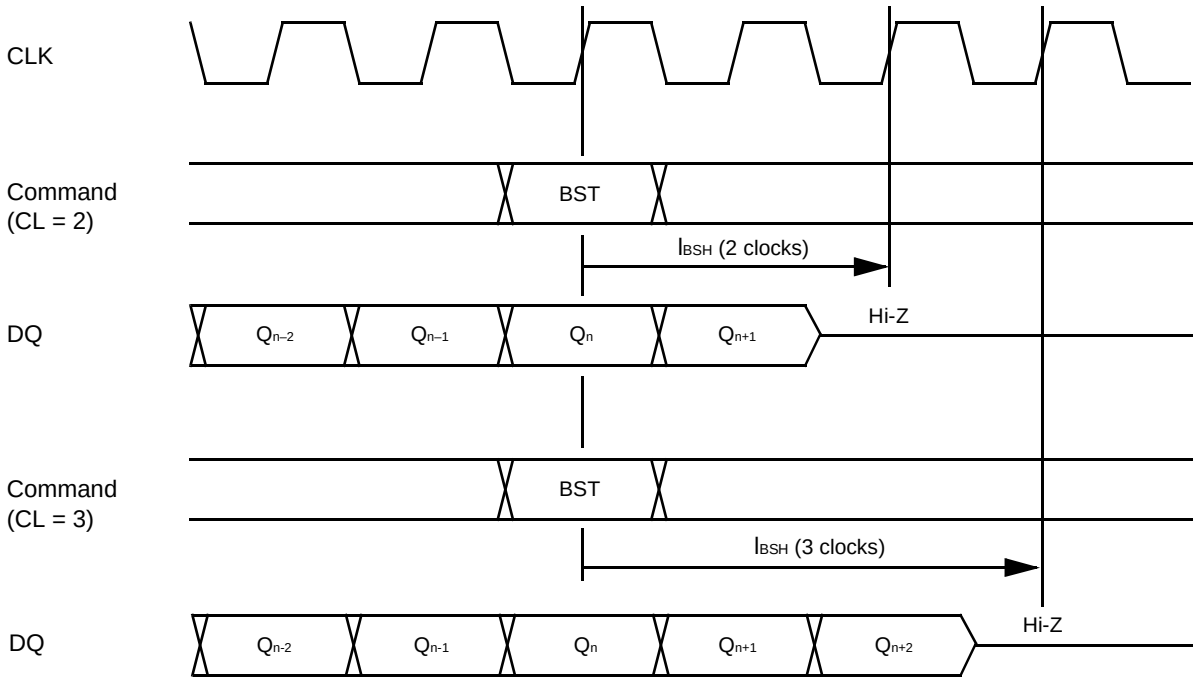


**TIMING DIAGRAM – 7 : READ INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 2, BL = 4)**

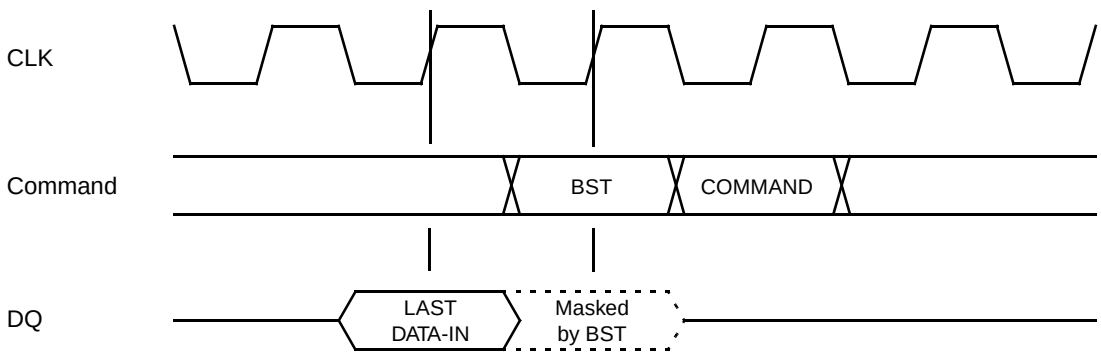



**Note:** In case of CL = 2, the $I_{ROH}$ is 2 clock.
In case of CL = 3, the $I_{ROH}$ is 3 clock.

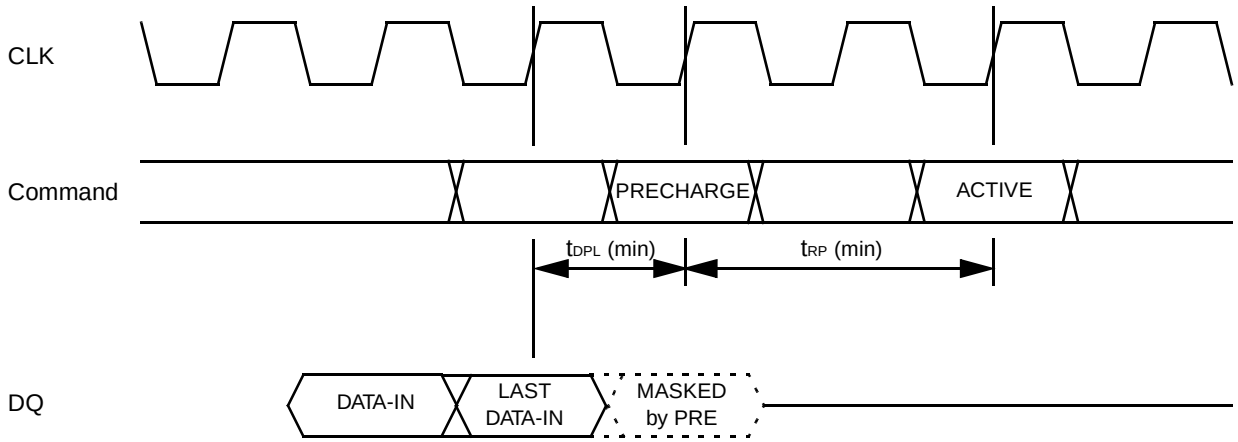
**TIMING DIAGRAM – 8 : READ INTERRUPTED BY BURST STOP (EXAMPLE @ BL = Full Column)**




**TIMING DIAGRAM – 9 : WRITE INTERRUPTED BY BURST STOP (EXAMPLE @ CL = 2)**

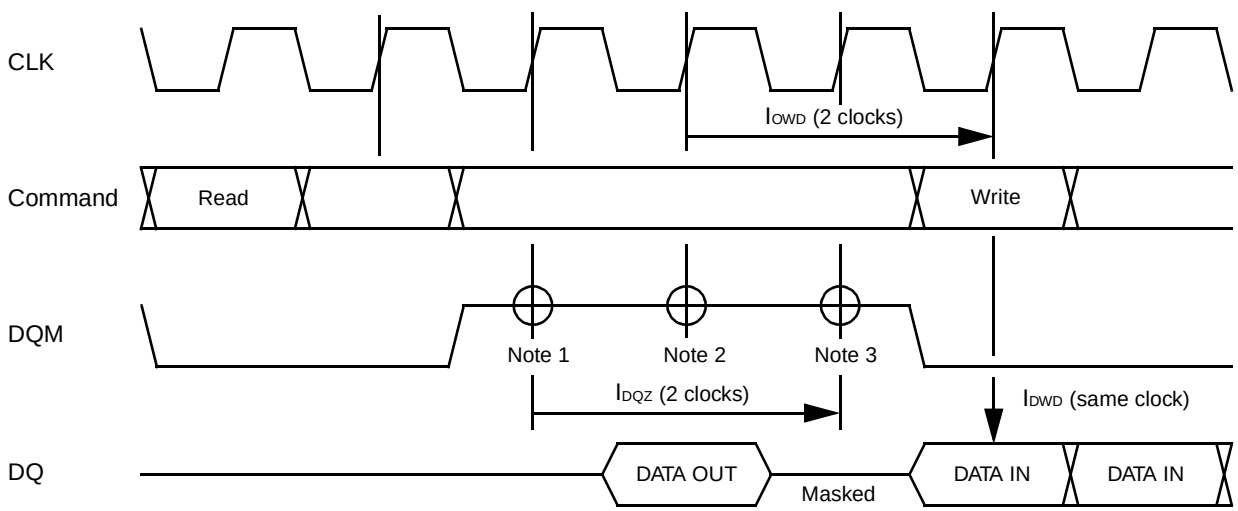


## TIMING DIAGRAM – 10 : WRITE INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 3)



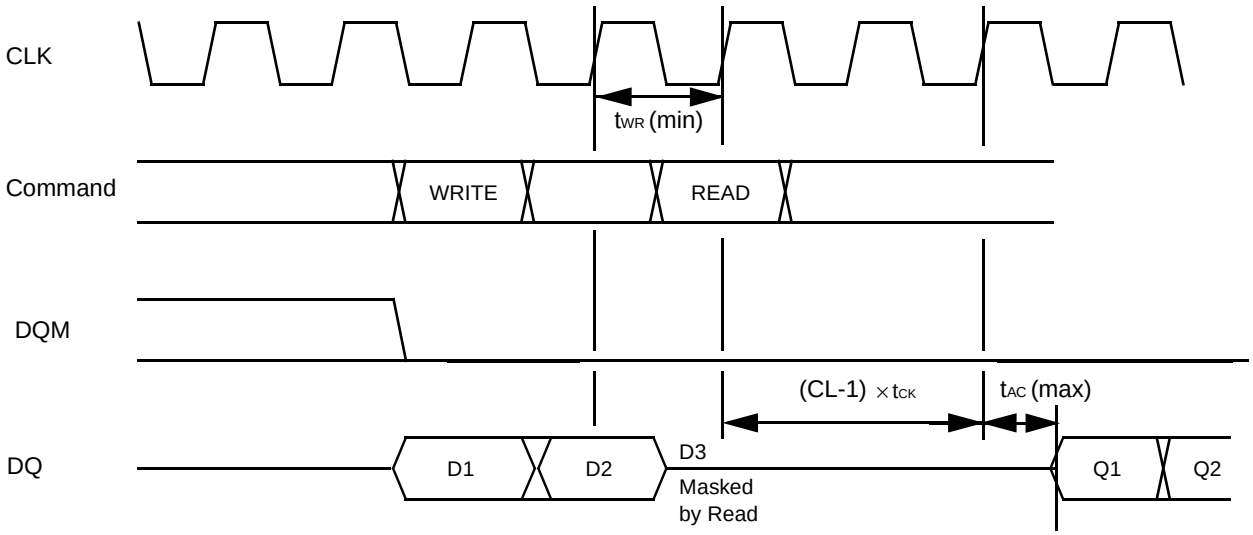

**Note:** The precharge command (PRE) should only be issued after the $t_{DPL}$ of final data input, is satisfied.

## TIMING DIAGRAM – 11 : READ INTERRUPTED BY WRITE (EXAMPLE @ CL = 3, BL = 4)



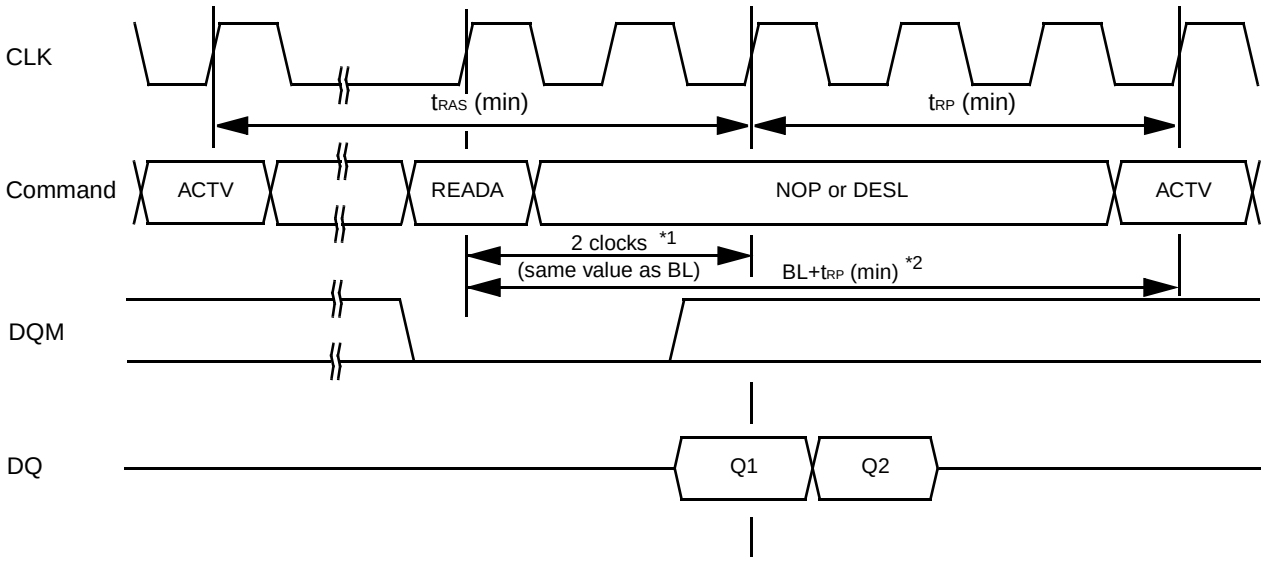

**Notes:** 1. First DQM makes high-impedance state High-Z between last output and first input data.
2. Second DQM makes internal output data mask to avoid bus contention.
3. Third DQM in illustrated above also makes internal output data mask. If burst read ends (final data output) at or after the second clock of burst write, this third DQM is required to avoid internal bus contention.

**TIMING DIAGRAM – 12 : WRITE TO READ TIMING (EXAMPLE @ CL = 3, BL = 4)**




**Note:** Read command should be issued after $t_{WR}$ of final data input is satisfied if read command is applied to the same bank.

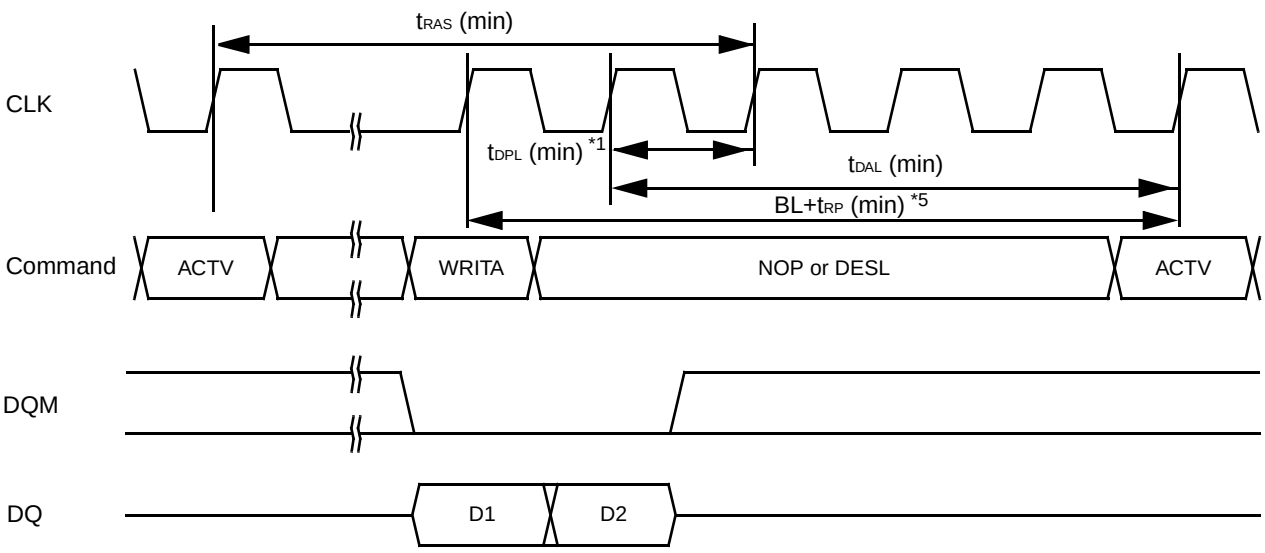
## TIMING DIAGRAM – 13 : READ WITH AUTO-PRECHARGE (EXAPLE @ CL = 2, BL = 2 Applied to same bank)




**Notes:** *1. Precharge at read with Auto-precharge command (READA) is started from number of clocks that is the same as Burst Length (BL) after the READA command is asserted.

*2. Next ACTV command should be issued after BL+$t_{RP}$ (min) from READA command.

## TIMING DIAGRAM – 14 : WRITE WITH AUTO-PRECHARGE (EXAMPLE @ CL = 2, BL = 2 Applied to same bank)




**Notes:** *1. Precharge at write with Auto-precharge is started after the $t_{DPL}$ from the end of burst.

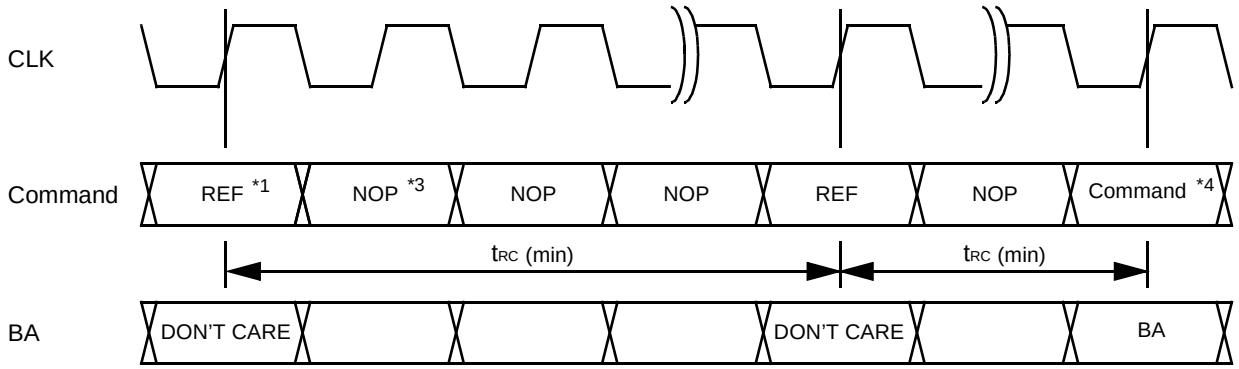
*2. Even if the final data is masked by DQM, the precharge does not start the clock of final data input.

*3. Once auto precharge command is asserted, no new command within the same bank can be issued.

*4. Auto-precharge command doesn't affect at full column burst operation except Burst READ & Single Write.

*5. Next command should be issued after BL+ $t_{RP}$ (min) at CL = 2, BL+1+$t_{RP}$ (min) at CL = 3 from WRITA command.

## TIMING DIAGRAM – 15 : AUTO-REFRESH TIMING



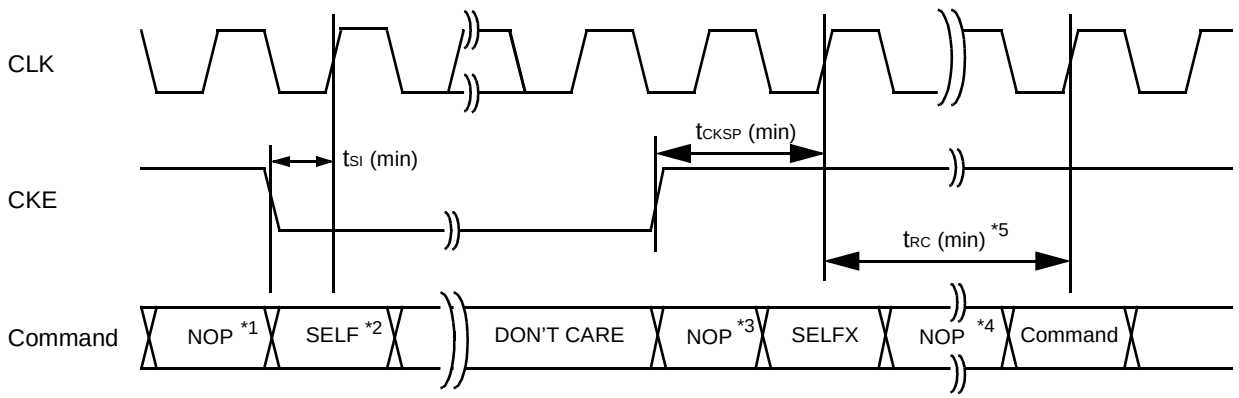

**Notes:** *1. All banks should be precharged prior to the first Auto-refresh command (REF).

*2. Bank select is ignored at REF command. The refresh address and bank select are selected by internal refresh counter.

*3. Either NOP or DESL command should be asserted during $t_{RC}$ period while Auto-refresh mode.

*4. Any activation command such as ACTV or MRS command other than REF command should be asserted after $t_{RC}$ from the last REF comand.

## TIMING DIAGRAM – 16 : SELF-REFRESH ENTRY AND EXIT TIMING




**Notes:** *1. Precharge command (PRE or PALL) should be asserted if any bank is active prior to Self-refresh Entry command (SELF).

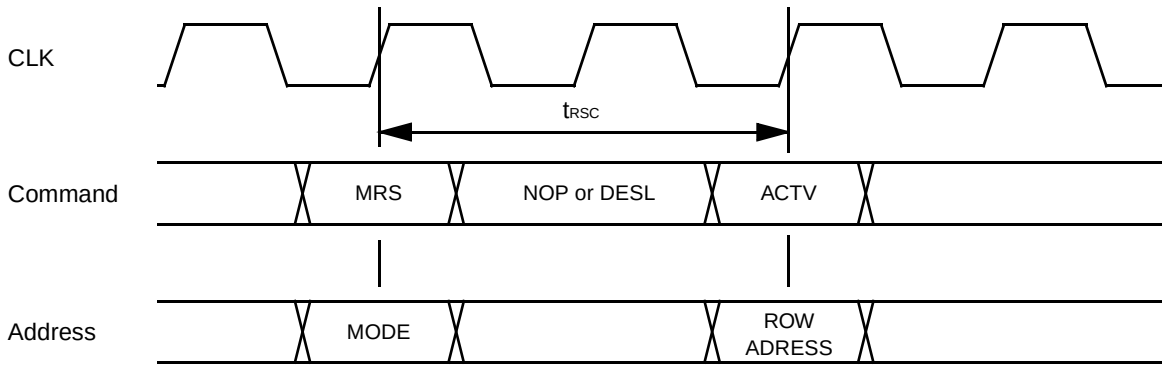
*2. SELF command should be asserted after the last read data have been appeared on DQ.

*3. The Self-refresh Exit command (SELFX) is latched after $t_{CKSP}$ (min). It is recommended to apply NOP command in conjunction with CKE.

*4. Either NOP or DESL command can be used during $t_{RC}$ period.

*5. CKE should be held high within one $t_{RC}$ period after $t_{CKSP}$.

## TIMING DIAGRAM – 17 : MODE REGISTER SET TIMING



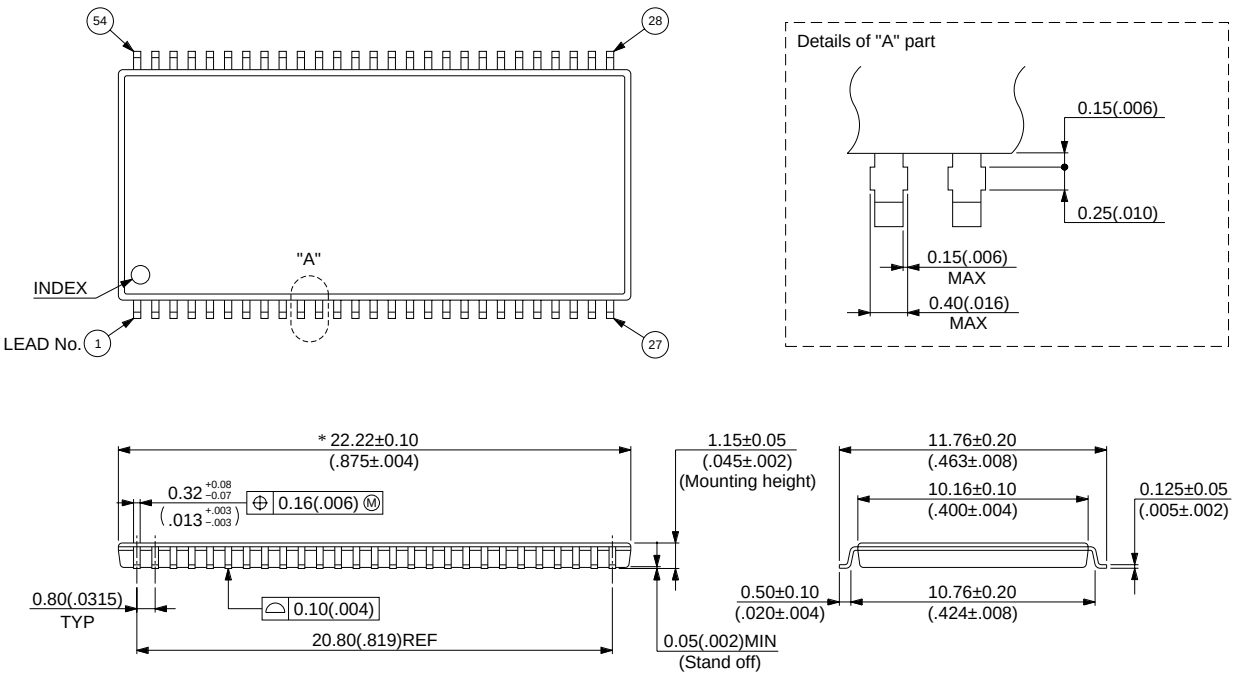

**Notes:** 1. The Mode Register Set command (MRS) should only be asserted after all banks have been precharged.
2. The MRS command should only be asserted on condition that DQ is in High-Z.

# MB81F64442B-103E/-103/-10/-103L/-10L

## ■ PACKAGE DIMENSION

54-pin plastic TSOP(II)
(FPT-54P-M02)

*: Resin protrusion. (Each side: 0.15 (.006) MAX)






Dimensions in mm (inches)

# FUJITSU LIMITED

*For further information please contact:*

**Japan**
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

*http://www.fujitsu.co.jp/*

**North and South America**
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 922-9179

Customer Response Center
*Mon. - Fri.: 7 am - 5 pm (PST)*
Tel: (800) 866-8608
Fax: (408) 922-9179

*http://www.fujitsumicro.com/*

**Europe**
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

*http://www.fujitsu-ede.com/*

**Asia Pacific**
FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

*http://www.fmap.com.sg/*

F9801




The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).
CAUTION:
Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.